

Compal Confidential

Model Name : V4DA2

File Name : LA-A131P

BOM P/N:43



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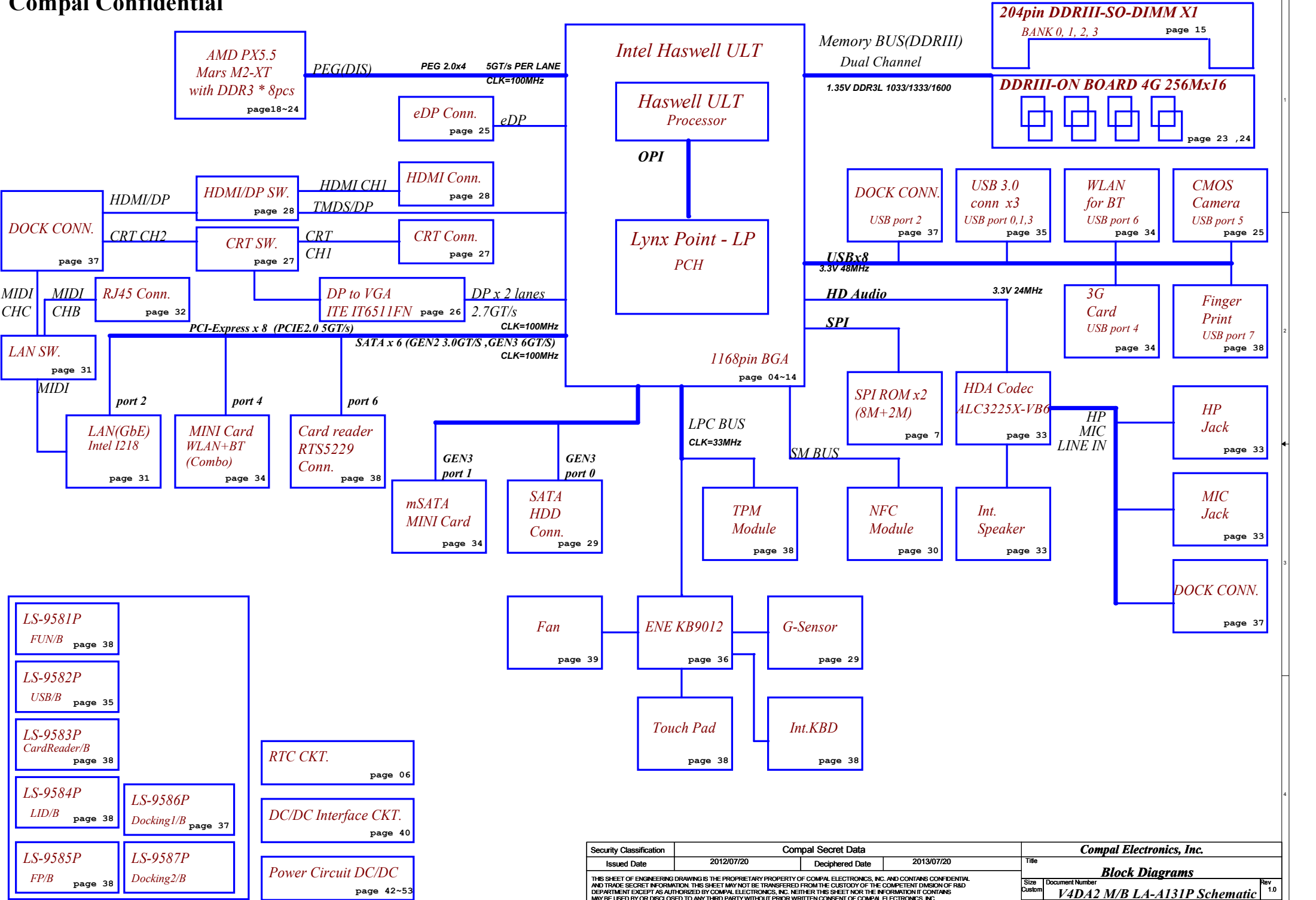
V4DA2 M/B Schematics Document

Haswell ULT Processor + Lynx Point - LP PCH+AMD Mars

2013-08-05

Rev:1.0

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Voltage Rails

Power Plane	Description	S0	S3	S4	S5	S3	S4	S5
+RTCVCC	RTC power	ON	ON	ON	ON	ON	ON	ON
VIN	Adapter power supply (19V)	N/A	ON	ON	ON	OFF	OFF	OFF
BATT+	Battery power supply (9V or 19V)	N/A	N/A	N/A	N/A	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW	+3VALW always on power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH	ON	ON	ON	ON	ON	ON	ON
+3VM	+3VALW to +3VM power rail for PCH	ON	ON*	ON*	ON*	ON*	ON*	ON*
+1.05VM	+1.05VS_VTT to +1.05VM switched power rail for CPU & PCH	ON	ON*	ON*	ON*	ON*	ON*	ON*
+1.05VS_VTT	+1.05VSP to +1.05VS_VTT switched power rail for CPU & PCH	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.35V	+1.35VP to +1.35V switched power rail for DDR terminator	ON	ON	OFF	OFF	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.8VSDGPU	+1.8VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+0.95VSDGPU	+1.8VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+3V_LAN	LAN CHIP POWER RAIL	ON*	ON*	ON*	OFF	OFF	OFF	OFF
+3VS_WLAN	WLAN MODULE POWER RAIL	ON*	ON*	ON*	OFF	OFF	OFF	OFF
+USB3_VCCA	USB Charger PORT0 & PORT9 POWER POWER RAIL	ON	ON	ON	ON	ON*	ON*	ON*

Note : ON* WILL DEPEND ON SLP_A# TO TURN ON OR OFF(ME FIRMWARE CONTROL)

Note : ON* WILL DEPEND ON BATTERY CAPACITY TO TURN ON OR OFF

Note : ON** Depend on Optimus ON/OFF.

Note : ON* Depend on LAN wake SPEC

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
On Board Thermal Sensor(CPU)	1001_101xb
On Board Thermal Senser(GPU)	1001_100xb
PCH	0100_1100b
	0100_1011b

PCH SM Bus address

Device	Address
ChannelA DIMM0	A0 1010 000Xb
ChannelB DIMM0	A4 1010 010Xb
G-sensor	0011 000xb

PCH SM Bus0 address

Device	Address
LAN	1100_100xb
NFC	0010_100xb

CPU BOM Config

0.8G	SA000067060 (S IC CL8064701325206 QDJB B1 0.8G BGA)
1.2G	SA00006G120 (S IC CL8064701325204 QDJ9 B1 1.2G BGA)

GPU BOM Config

MARS-XT-M2	SA000061J10 (S IC 216-0842000 A0 MARS XT M2 FCBGA 0FA)
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VRAM BOM Config

HYNIX	128*16	SA00003Y090(S IC D3 128M16 H5TQ2G63DFR-11C FBGA ABO!)	HYNIX0@
HYNIX	128*16	SA00006H430(S IC D3 128M16 H5TC2G63FFR-11C FBGA ABO!)	HYNIX1@

RAM BOM Config

ELPDIA	256*16	SA000059110(S IC D3 256M16 EDJ4216EBBG-DJ-F ABO!)	ELP0@
ELPDIA	256*16	SA00005HT50(S IC 256MX16/1600 EDJ4216EFBG-GN-F FBGA 96P ABO !)	ELP1@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S0 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

USB Port Table

USB 2.0	Port	USB Port
EHCI	0	USB Port 3.0 (I/O board)
	1	USB port 3.0 (Left side)
	2	DOCK USB3.0
	3	USB Port 3.0 (I/O board)
	4	Mini Card(3G)
	5	Camera
	6	Mini Card(WLAN+BT)
	7	Finger Print

USB 3.0	Port	
XHCI	1	USB Port 3.0 (I/O board)
	2	USB3 (Left side)

PCIe Table

Port	PCI Express Port
1	USB 3.0 DOCK
2	USB 3.0 (I/O board)
3	LAN
4	WLAN
5-L0	VGA
5-L1	
5-L2	
5-L3	
6-L0	CardReader

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

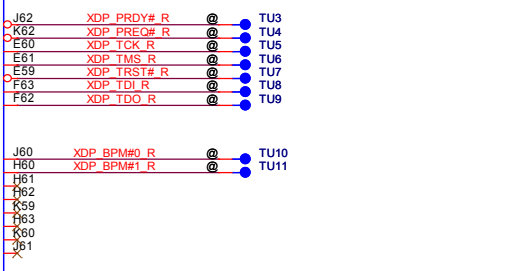
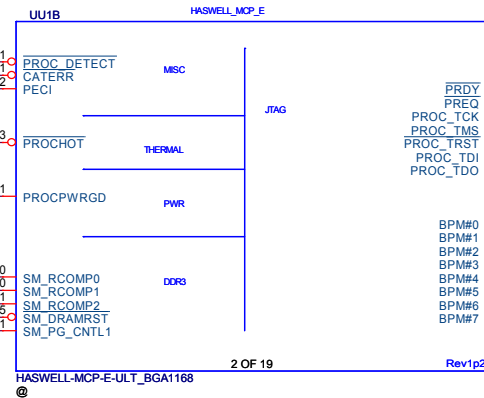
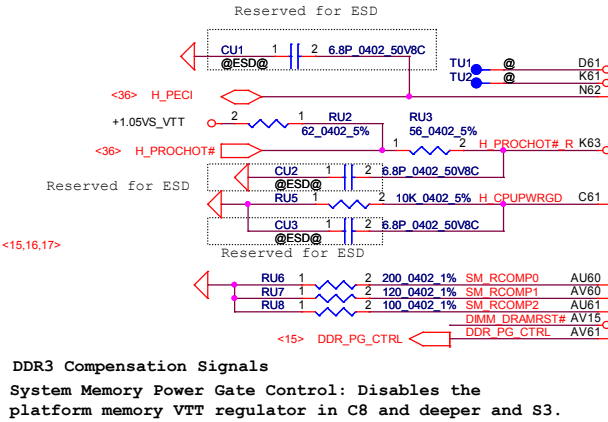
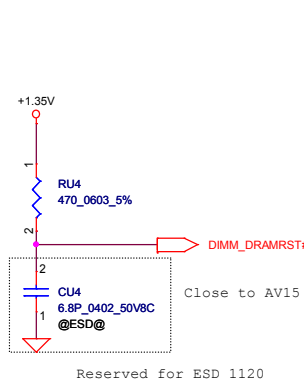
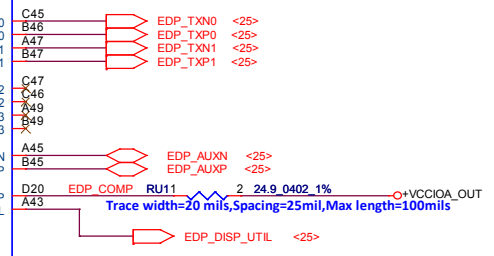
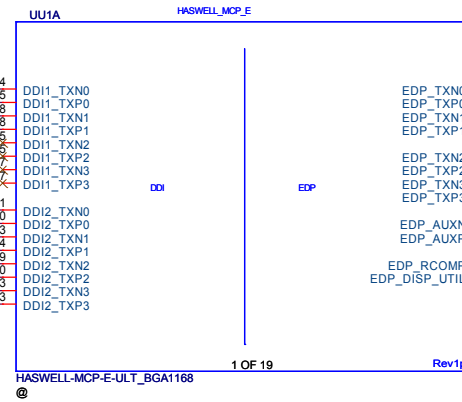
BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA Only	UMA@
DISCRETE	VGA@
CPU	
CPU	
CPU	
DRAM ELPIDA0	ELP0@
DRAM HYNIXR0	HYNIXR0@
NFC Function	NFC@
3G Function	3G@
VPRO Function	VPRO@
NO VPRO Function	NOVPRO@
EMI SOLUTION	EMI@
UMA Part Count	PC@
VGA Part Count	VGAPC@
ESD SOLUTION	ESD@
VRAM HYNIX0	HYNIX0@
VRAM HYNIX1	HYNIX1@

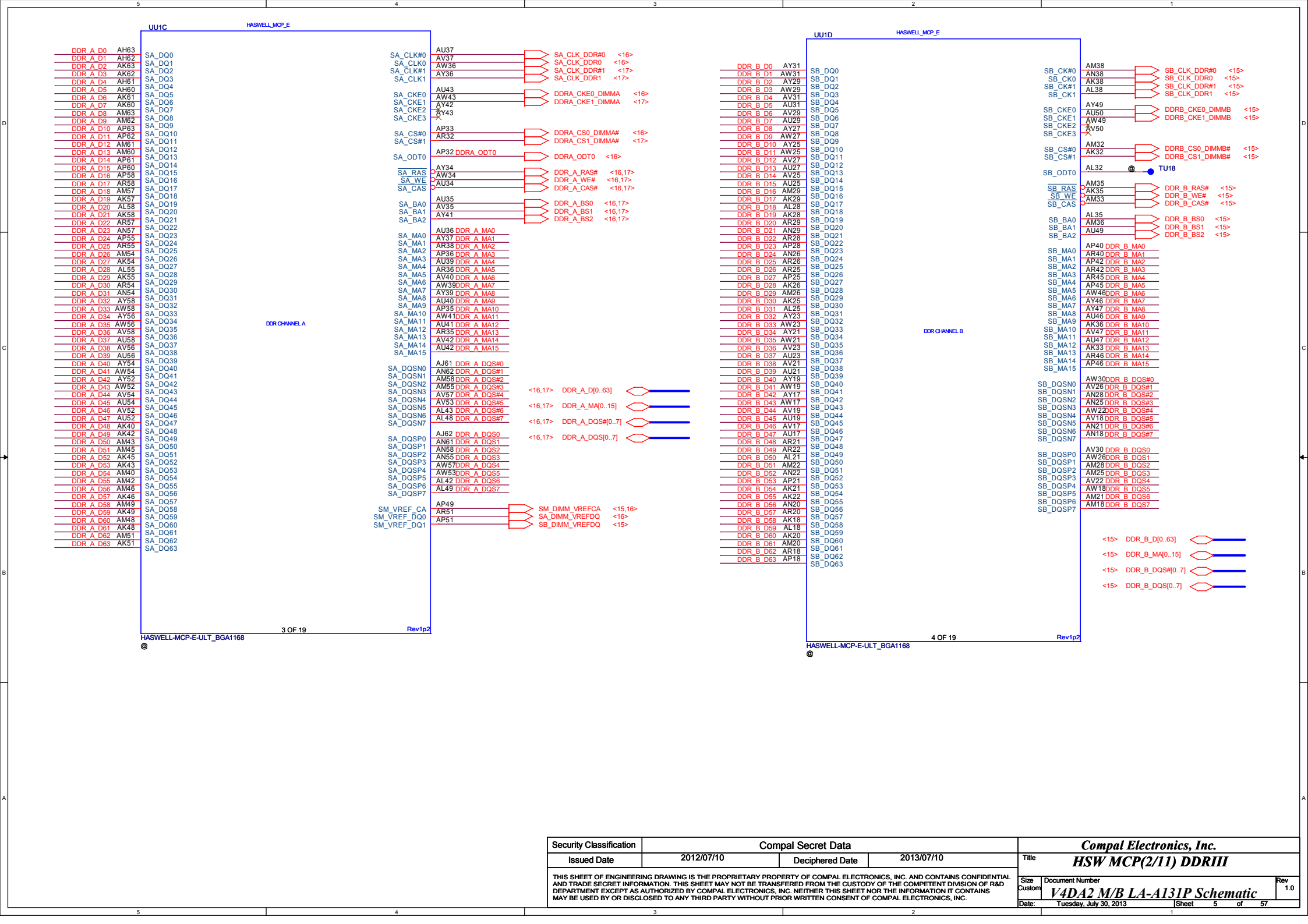
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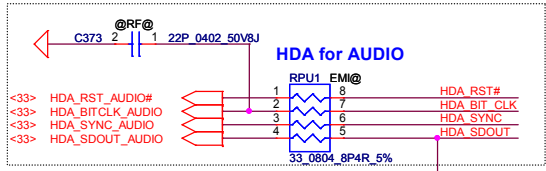
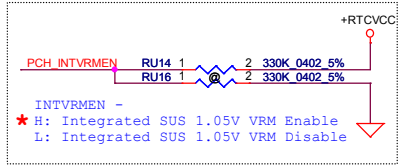
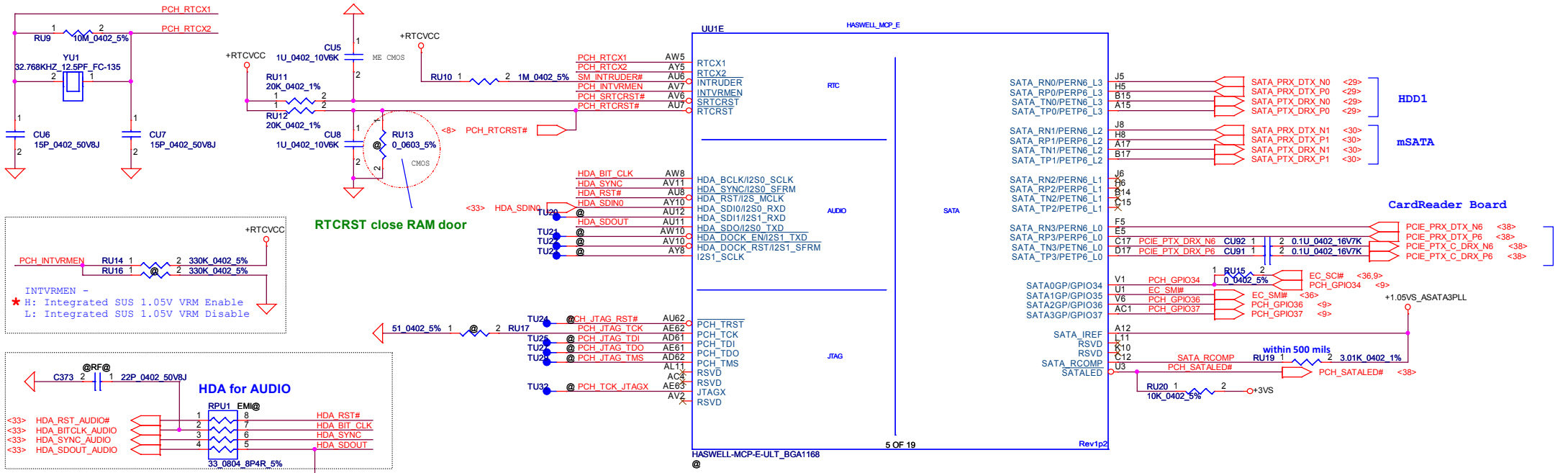
DP to CRT

HDMI

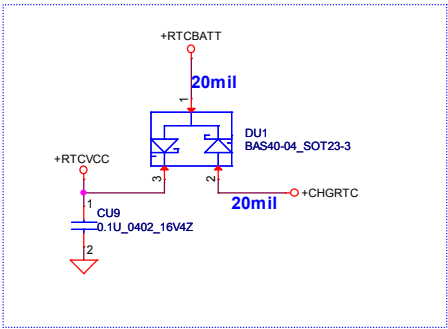


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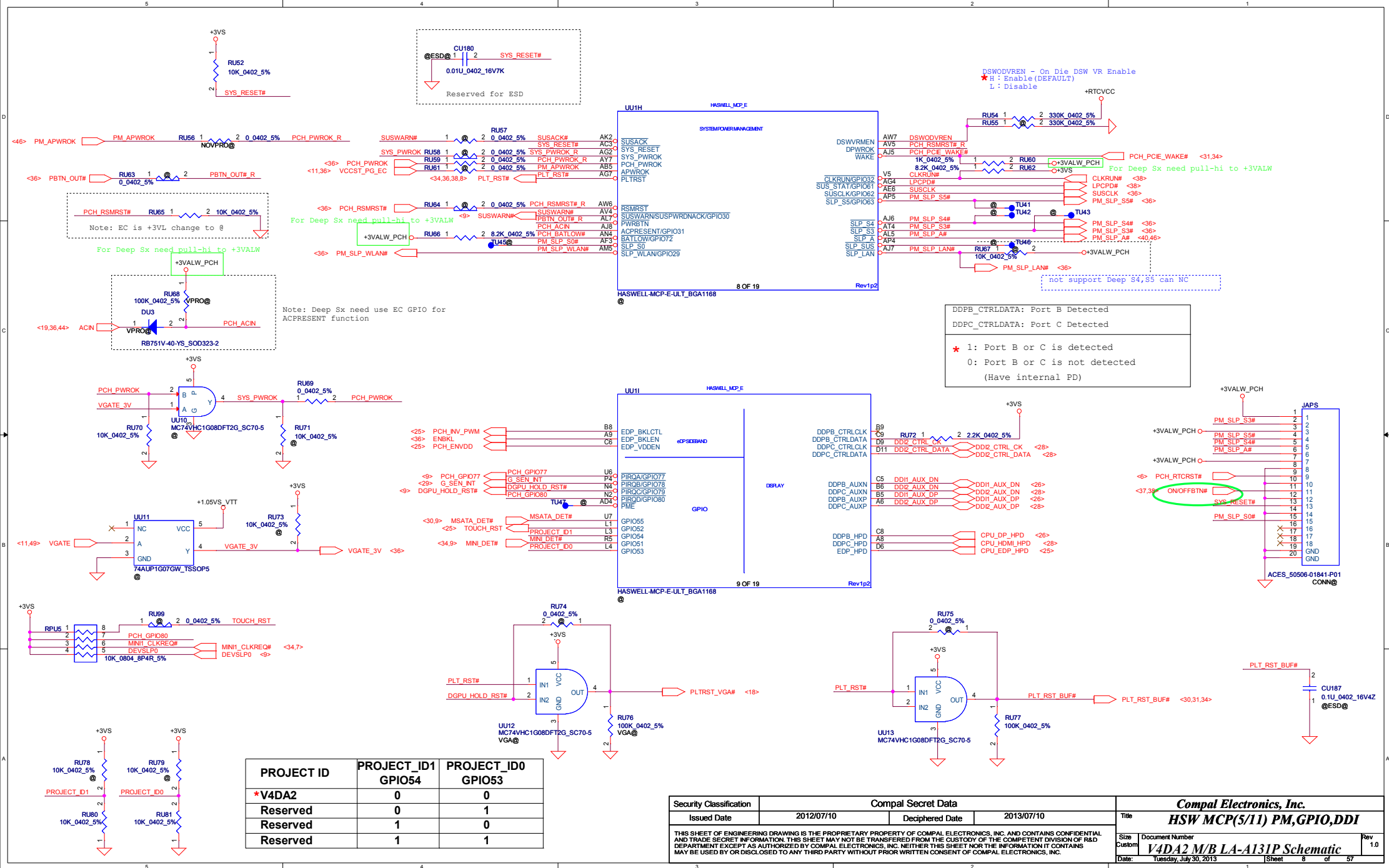


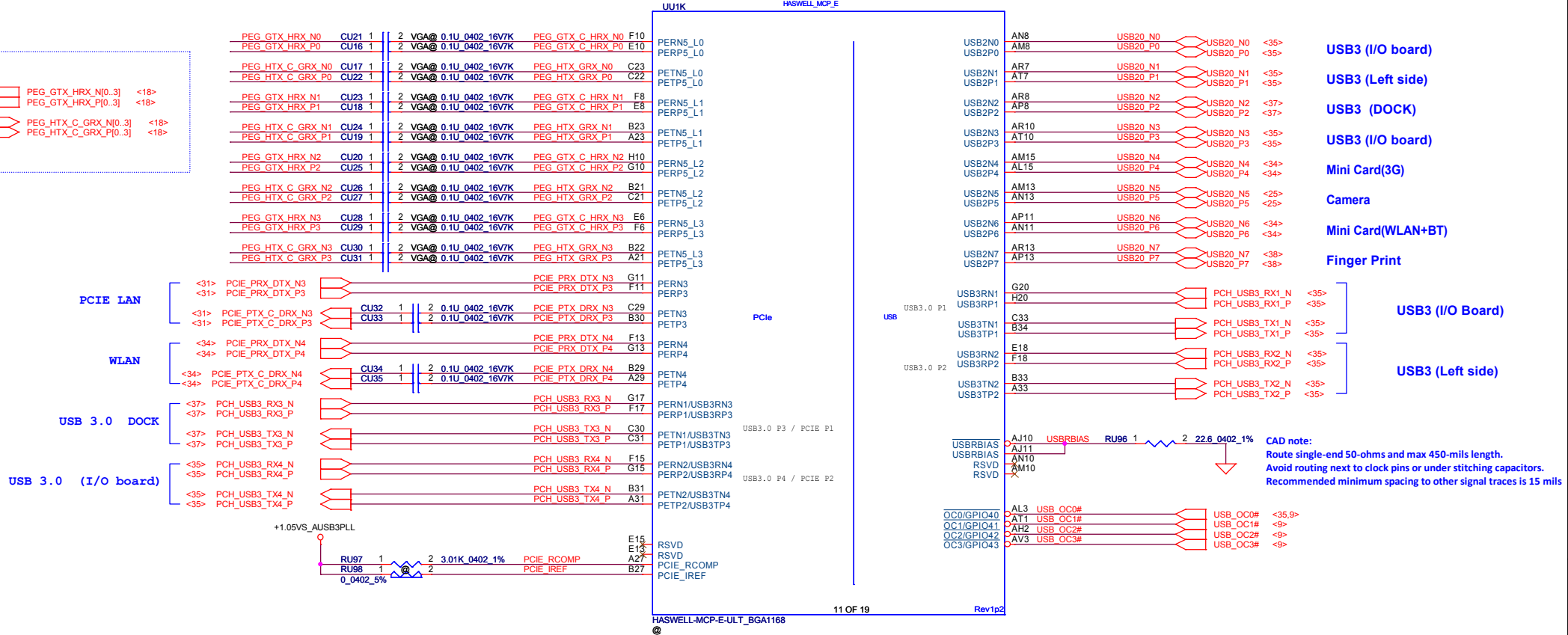
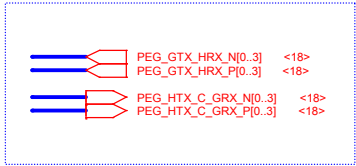


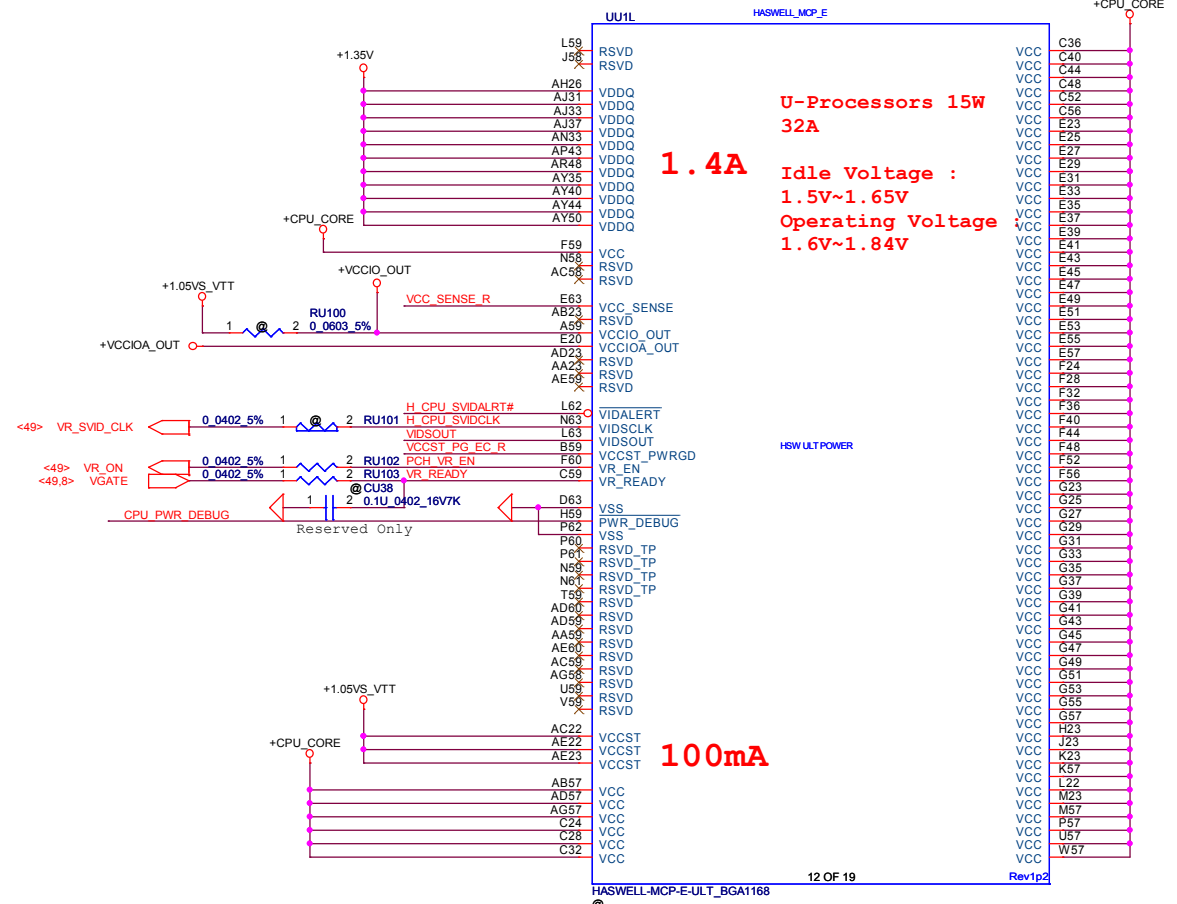
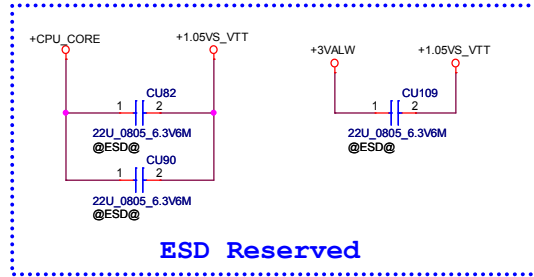
ME Debug (internal pull-down)
1: Disable Flash Descriptor Security (override)



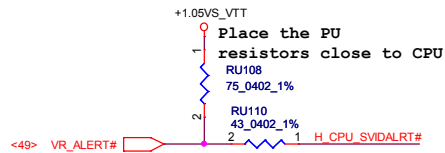
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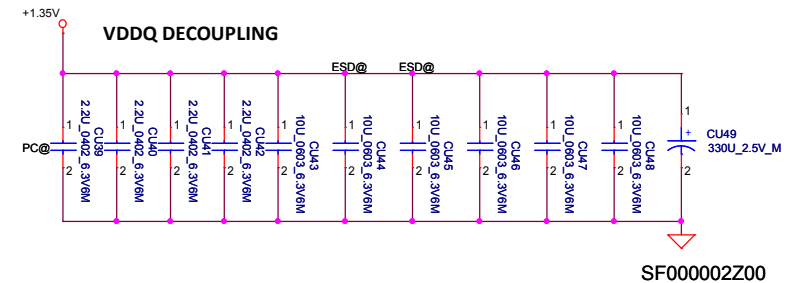
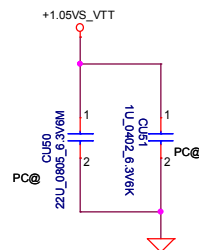
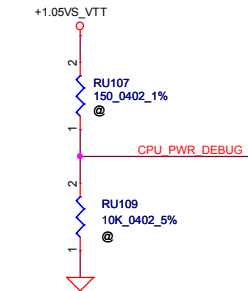
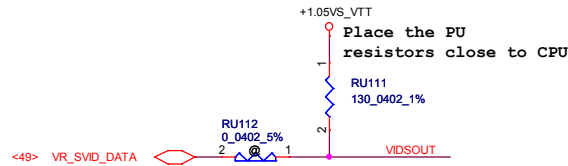




SVID ALERT



SVID DATA

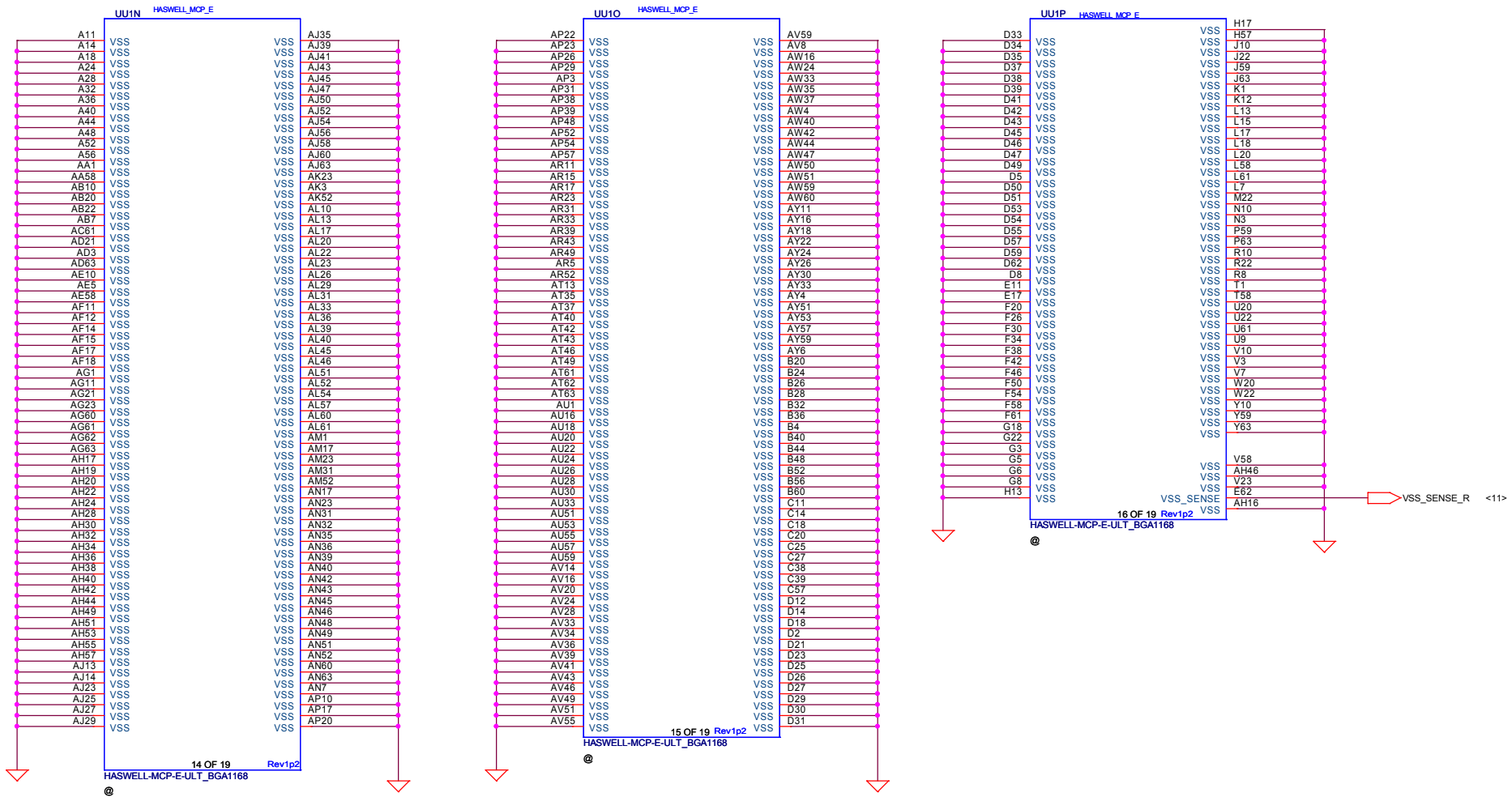


+1.35V : 470UF/2V/7343 *2

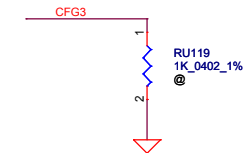
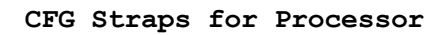
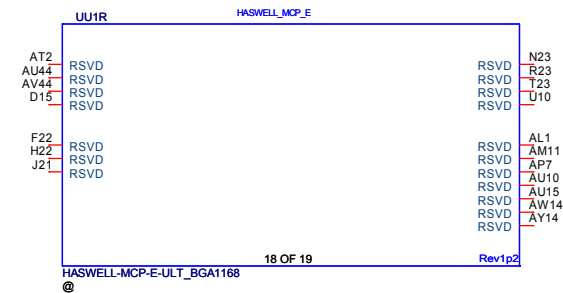
10UF/6.3V/0603 * 6

2.2UF/6.3V/0402 * 4

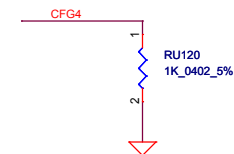
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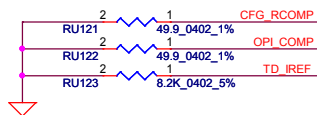
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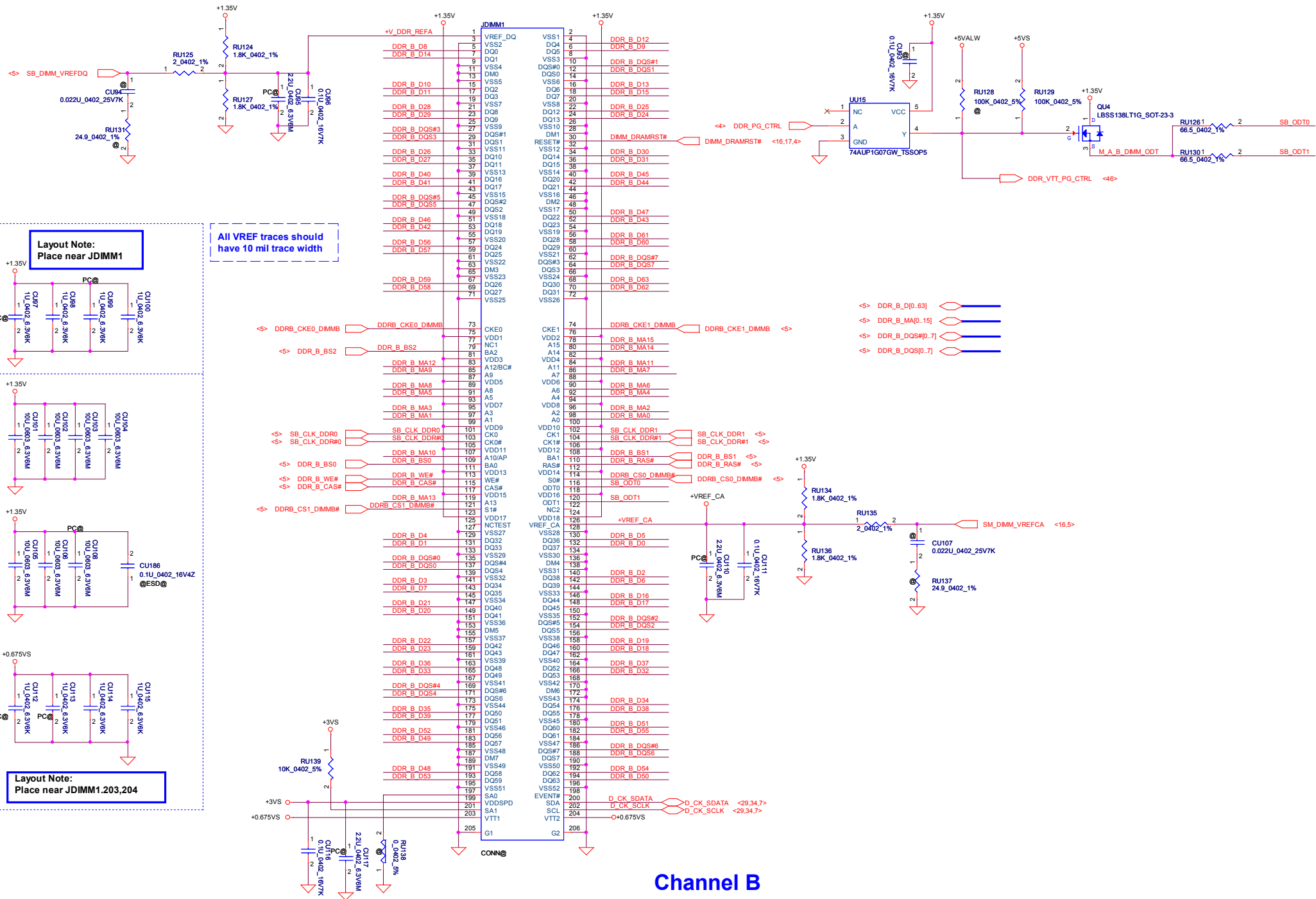


Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



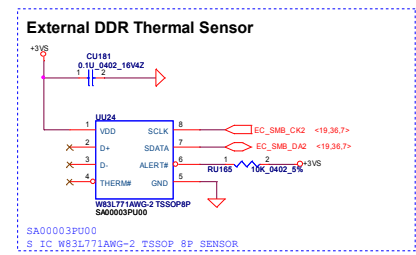
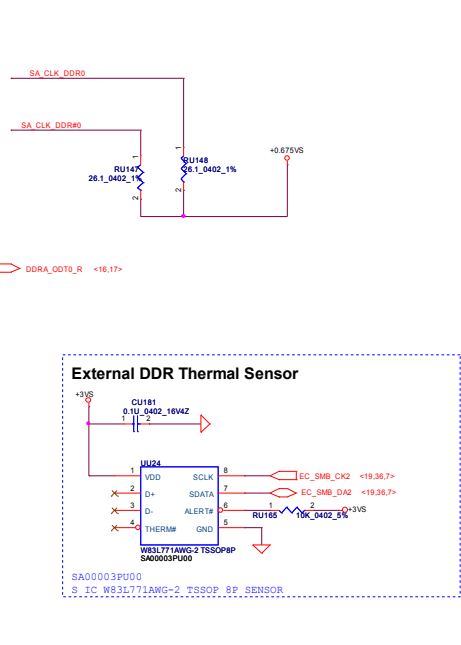
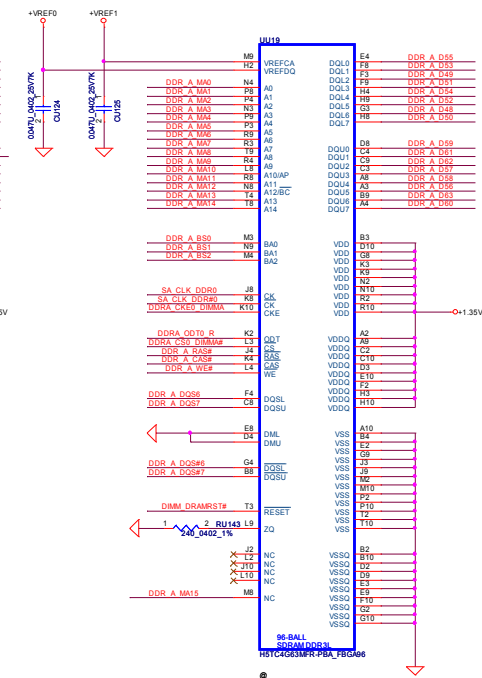
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



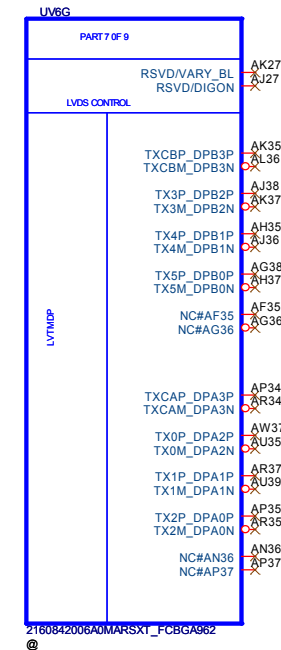
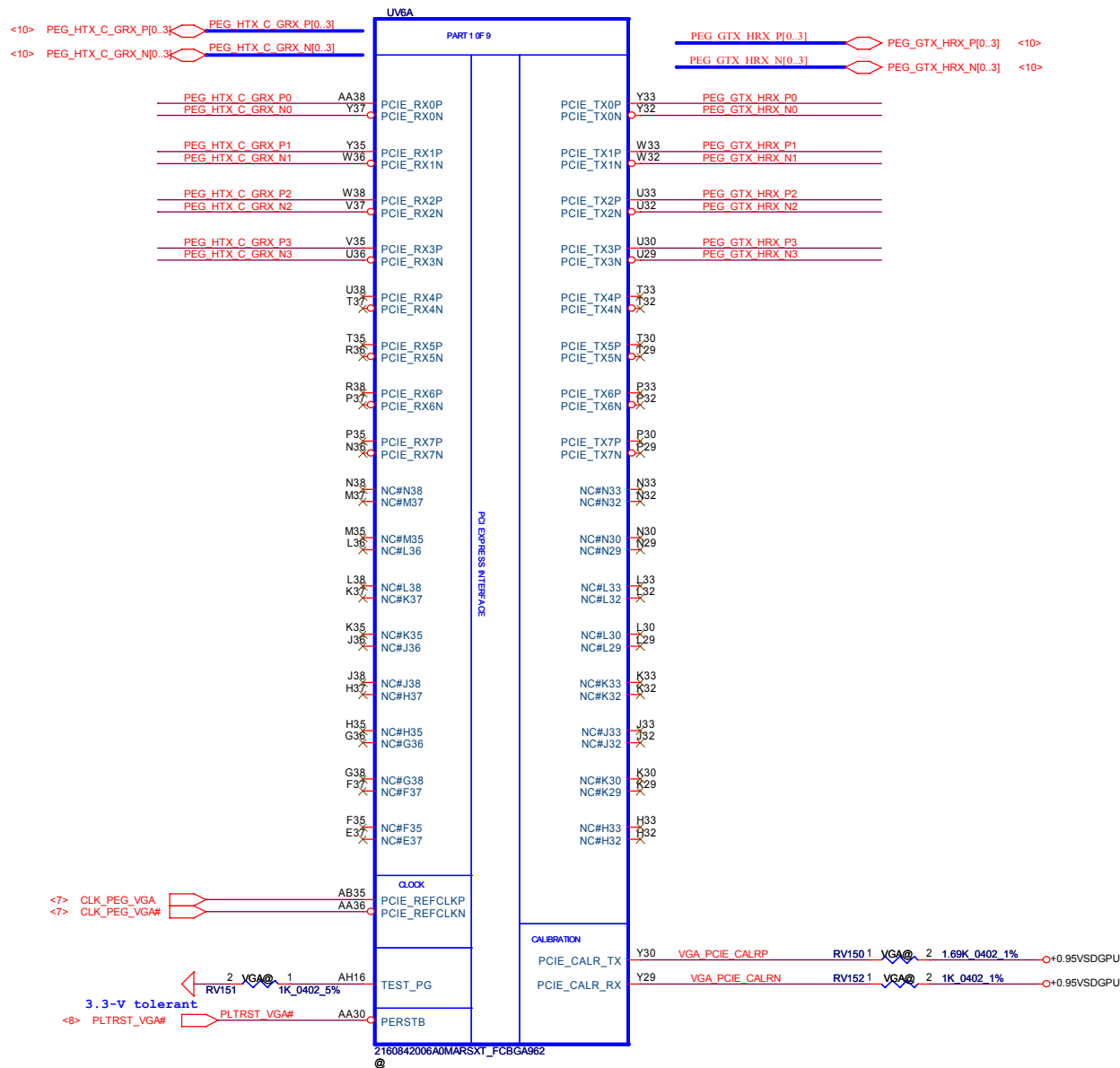


Channel B

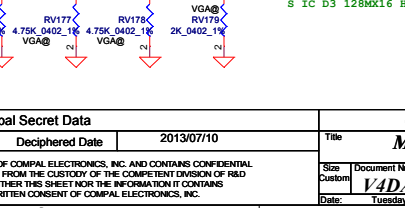
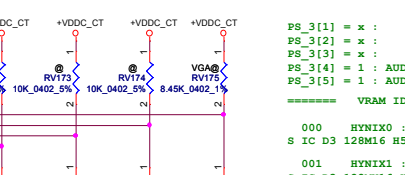
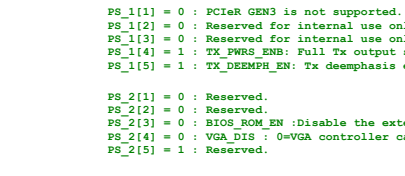
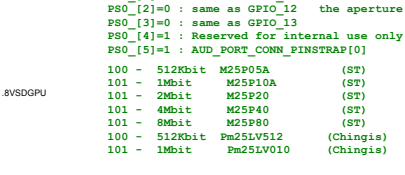
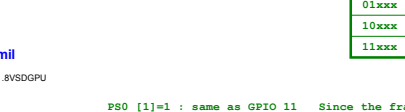
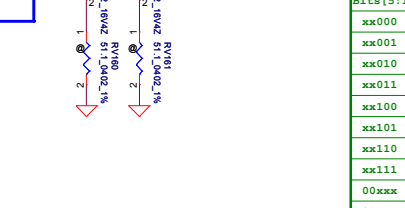
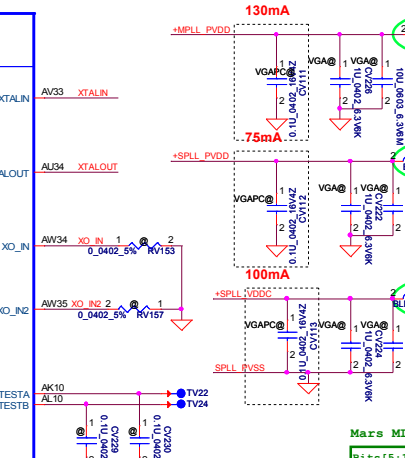
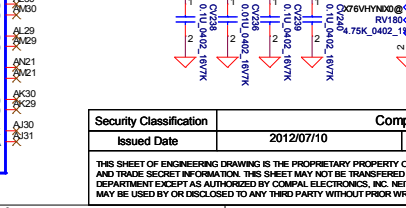
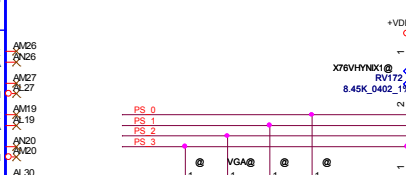
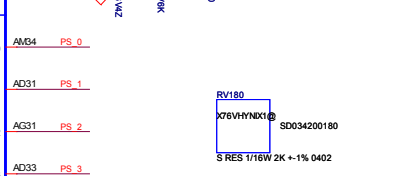
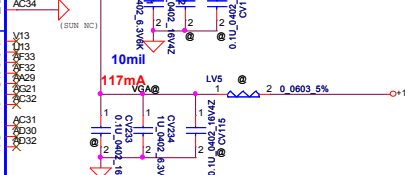
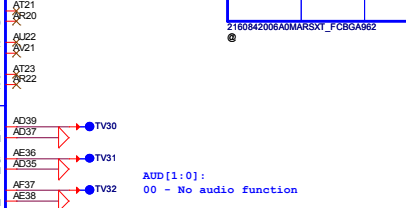
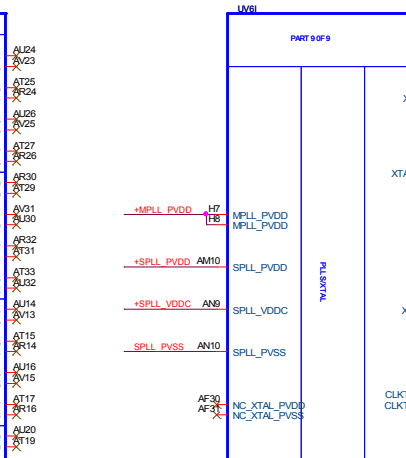
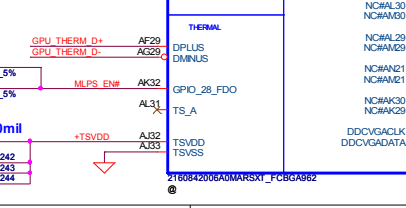
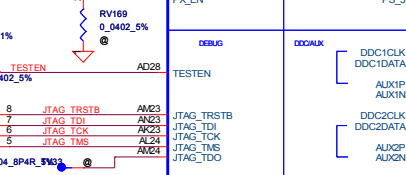
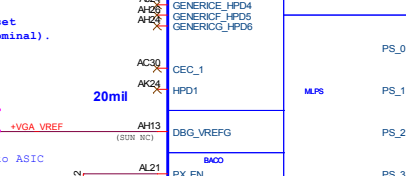
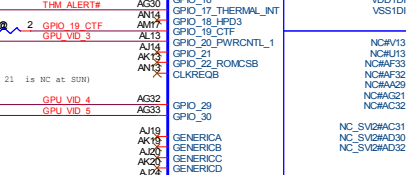
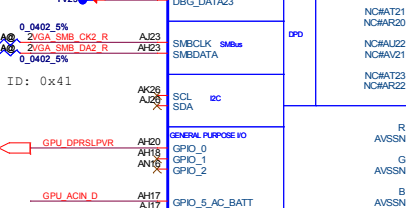
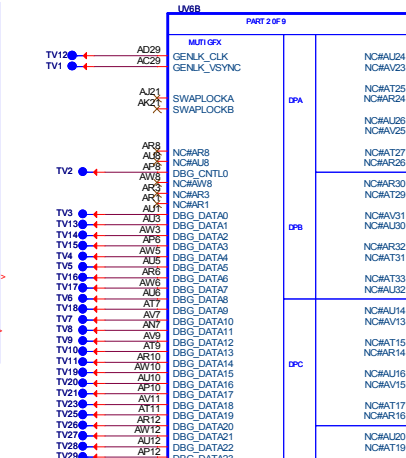
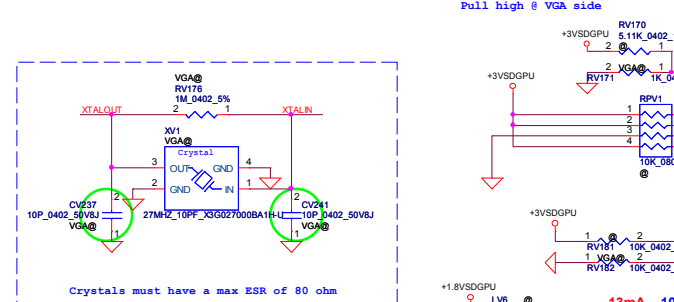
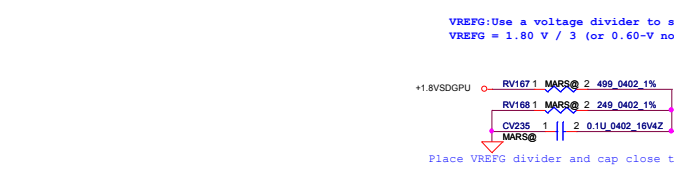
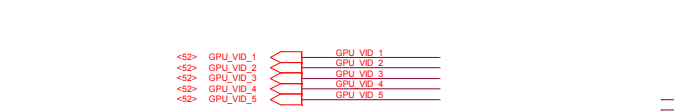
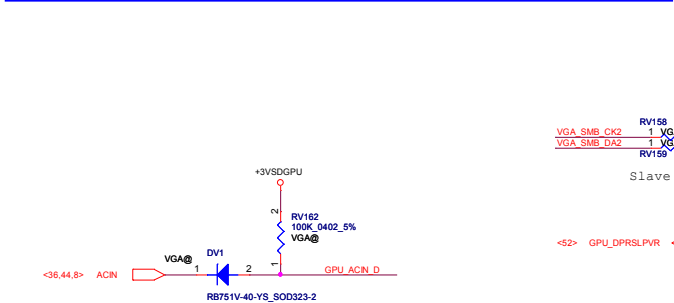
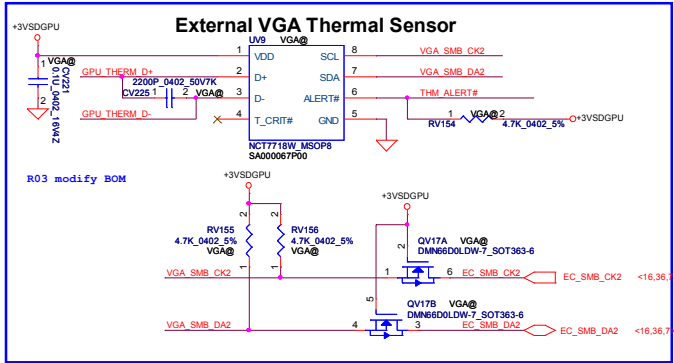
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GFX PCIE LANE REVERSAL



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		Deciphered Date		MARS-Pro_PCIE	
				Size Custom	
				Document Number	
				V4DA2 M/B LA-A131P Schematic	
				Date	
				Thursday, August 01, 2013	
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				Rev 1.0	



Mars MLPS configuration

Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

PS0[1]=1: same as GPIO 11 Since the frame buffer size is 512 MB
 PS0[2]=0: same as GPIO 12 the aperture size is set to 256 MB.
 PS0[3]=0: same as GPIO 13
 PS0[4]=1: Reserved for internal use only. Must be 1
 PS0[5]=1: AUD_PORT_CONN_PINSTRAP[0]

100 = 512Kbit M25P05A (ST)
 101 = 1Mbit M25P10A (ST)
 102 = 2Mbit M25P20 (ST)
 103 = 4Mbit M25P40 (ST)
 104 = 8Mbit M25P80 (ST)
 105 = 512Kbit Pm25LV512 (Chingis)
 106 = 1Mbit Pm25LV010 (Chingis)

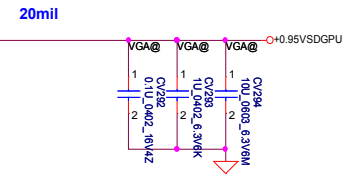
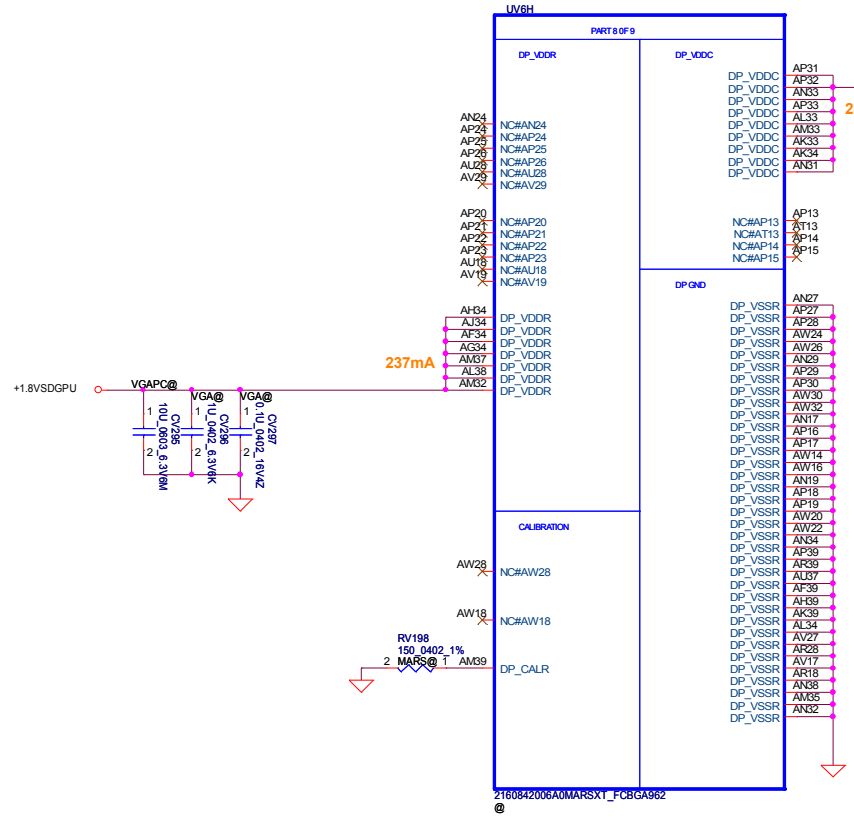
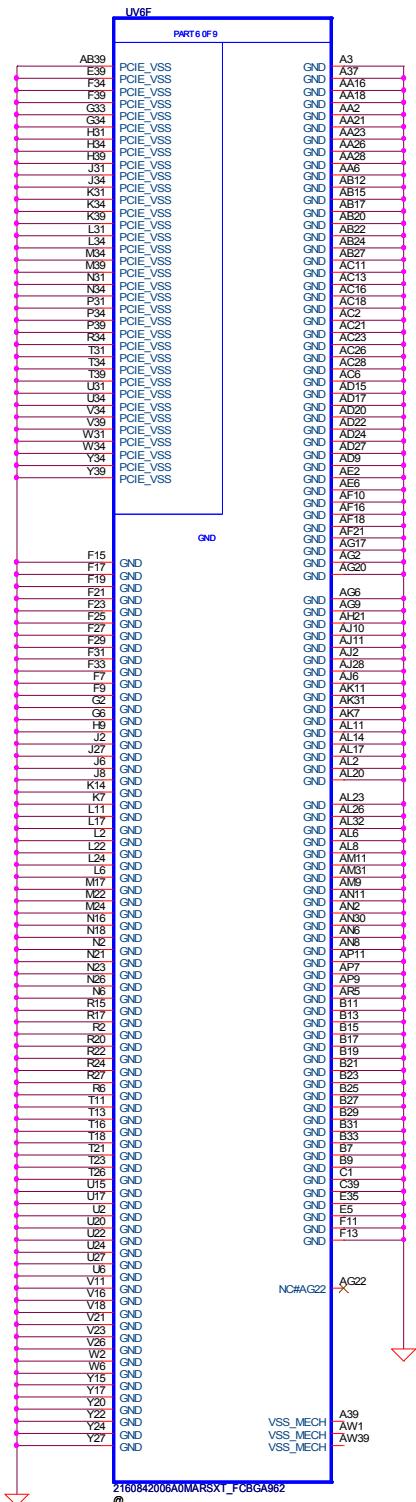
PS_1[1] = 0: PCIeR GEN3 is not supported.
 PS_1[2] = 0: Reserved for internal use only
 PS_1[3] = 0: Reserved for internal use only
 PS_1[4] = 1: TX_PWRS_ENB: Full Tx output swing.
 PS_1[5] = 1: TX_DEEMPH_EN: Tx deemphasis enabled.

PS_2[1] = 0: Reserved.
 PS_2[2] = 0: Reserved.
 PS_2[3] = 0: BIOS_ROM_EN: Disable the external BIOS ROM device.
 PS_2[4] = 0: VGA_DIS = 0:VGA controller capacity enabled.
 PS_2[5] = 1: Reserved.

PS_3[1] = x: VRAM ID
 PS_3[2] = x: VRAM ID
 PS_3[3] = x: VRAM ID
 PS_3[4] = 1: AUD_PORT_CONN_PINSTRAP[1]
 PS_3[5] = 1: AUD_PORT_CONN_PINSTRAP[2]
 ===== VRAM ID for Mars =====

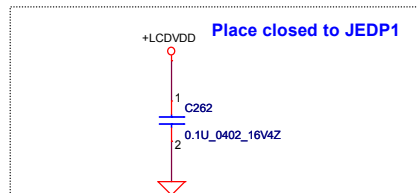
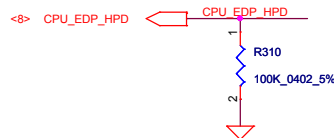
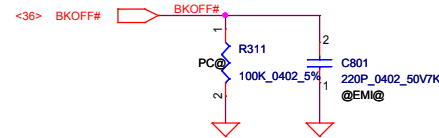
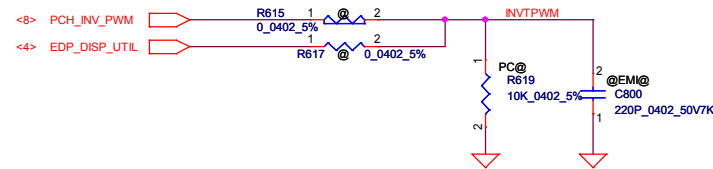
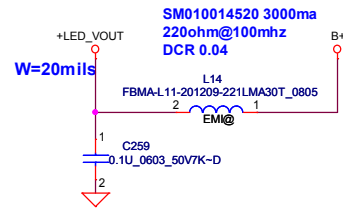
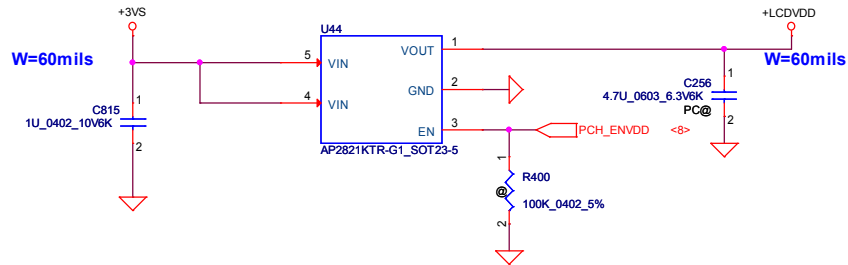
000 HYNIX0: SA00003Y090
 S IC D3 128M16 H57Q2663DPR-11C FBGA ABO!
 001 HYNIX1: SA00006H430
 S IC D3 128M16 H57C2663DPR-11C FBGA 96P ABO !

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Size	Document Number	Rev	
Custom	V4DA2 M/B LA-A131P Schematic	1.0	
Date:	Tuesday, July 30, 2013	Sheet	18 of 57

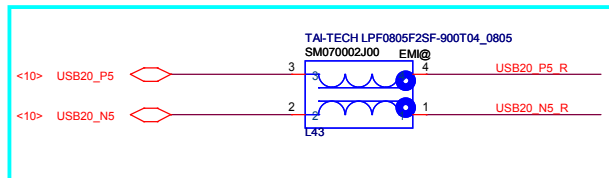


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		Custom		V4DA2 M/B LA-A131P Schematic	
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		Sheet		22 of 57	
		Rev		1.0	

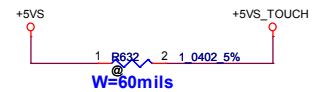
LCD POWER CIRCUIT



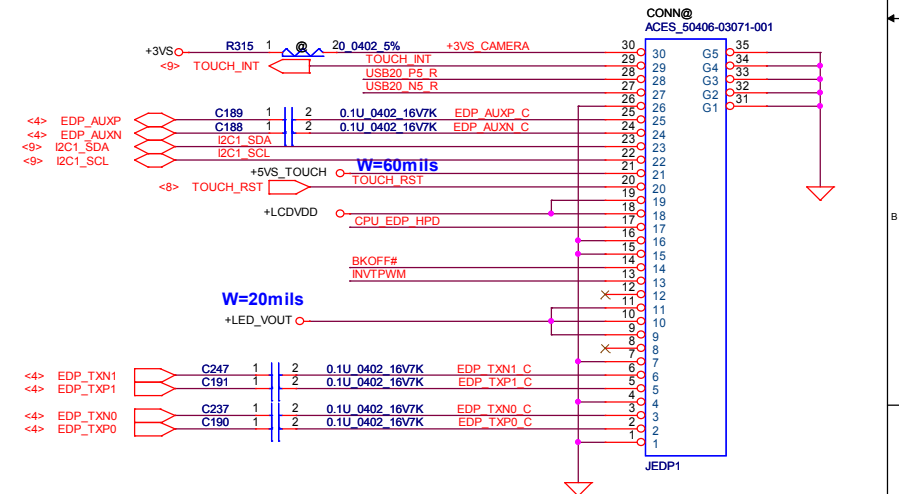
Camera



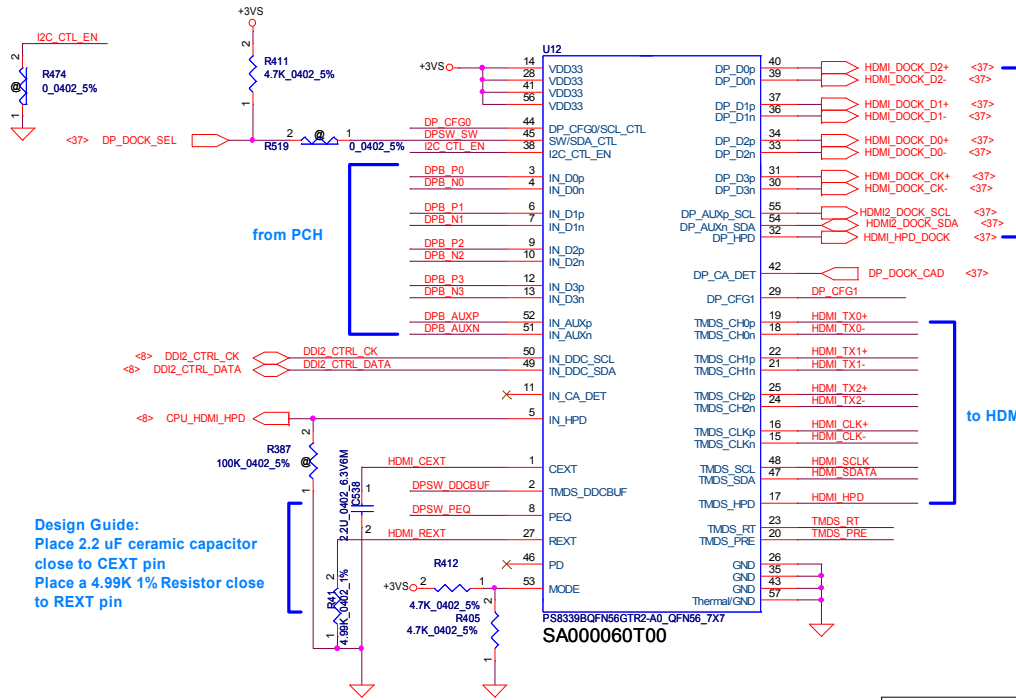
(EMI request)



eDP PANEL Conn.



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						Size	Document Number			Rev
						Custom	V4DA2 M/B LA-A131P Schematic			1.0
						Date:	Tuesday, July 30, 2013		Sheet	25 of 57

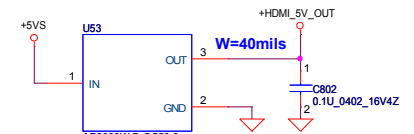
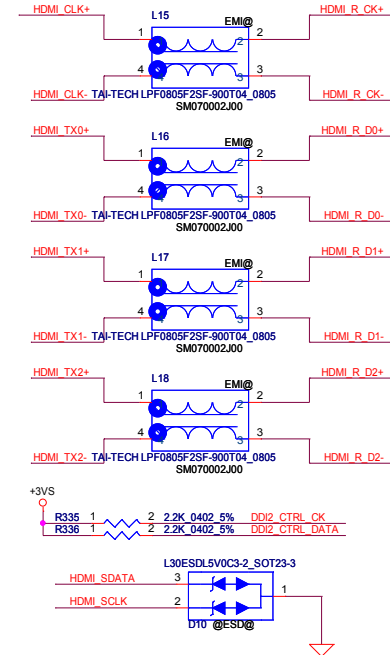
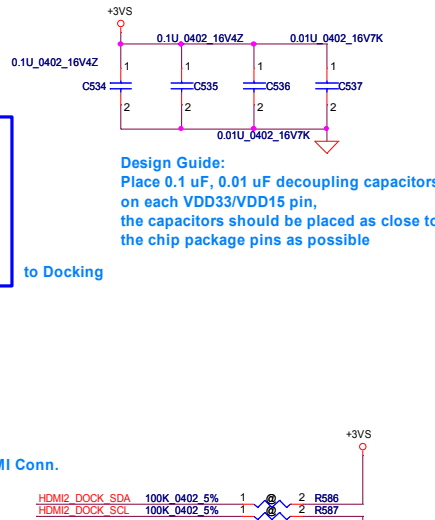


I2C_CTL_EN	Mode
Low	Pin Control Mode
High	I2C Control Mode

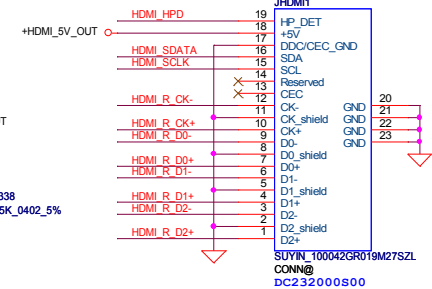
Control Switching Mode			
SW	DP Output	HDMI Output	HPD_SRC
0	Enable	Z	DP HPD
1	Z	Enable	HDMI HPD

AUTOSW_EN	Power Mode
Low	Control port switching
High	Automatic port switching

<4>	CPU_DP2_N0	CPU_DP2_N0	C268	2	1	0.1U_0402_16V7K	DPB_N0
<4>	CPU_DP2_P0	CPU_DP2_P0	C269	2	1	0.1U_0402_16V7K	DPB_P0
<4>	CPU_DP2_N1	CPU_DP2_N1	C270	2	1	0.1U_0402_16V7K	DPB_N1
<4>	CPU_DP2_P1	CPU_DP2_P1	C271	2	1	0.1U_0402_16V7K	DPB_P1
<4>	CPU_DP2_N2	CPU_DP2_N2	C272	2	1	0.1U_0402_16V7K	DPB_N2
<4>	CPU_DP2_P2	CPU_DP2_P2	C273	2	1	0.1U_0402_16V7K	DPB_P2
<4>	CPU_DP2_N3	CPU_DP2_N3	C274	2	1	0.1U_0402_16V7K	DPB_N3
<4>	CPU_DP2_P3	CPU_DP2_P3	C275	2	1	0.1U_0402_16V7K	DPB_P3
<8>	DDI2_AUX_DN	DDI2_AUX_DN	C283	2	1	0.1U_0402_16V7K	DPB_AUXN
<8>	DDI2_AUX_DP	DDI2_AUX_DP	C288	2	1	0.1U_0402_16V7K	DPB_AUXP

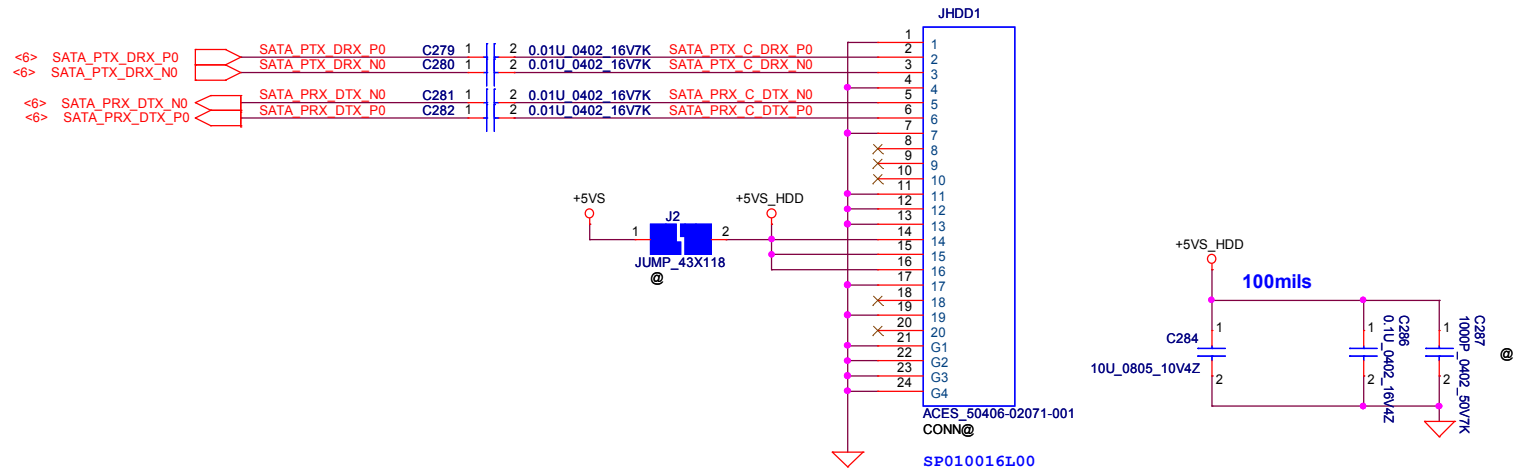


HDMI connector

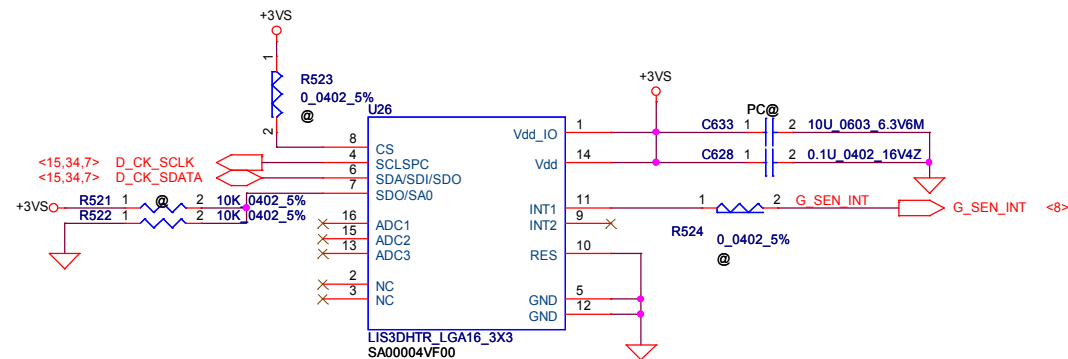


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HDD Board Conn

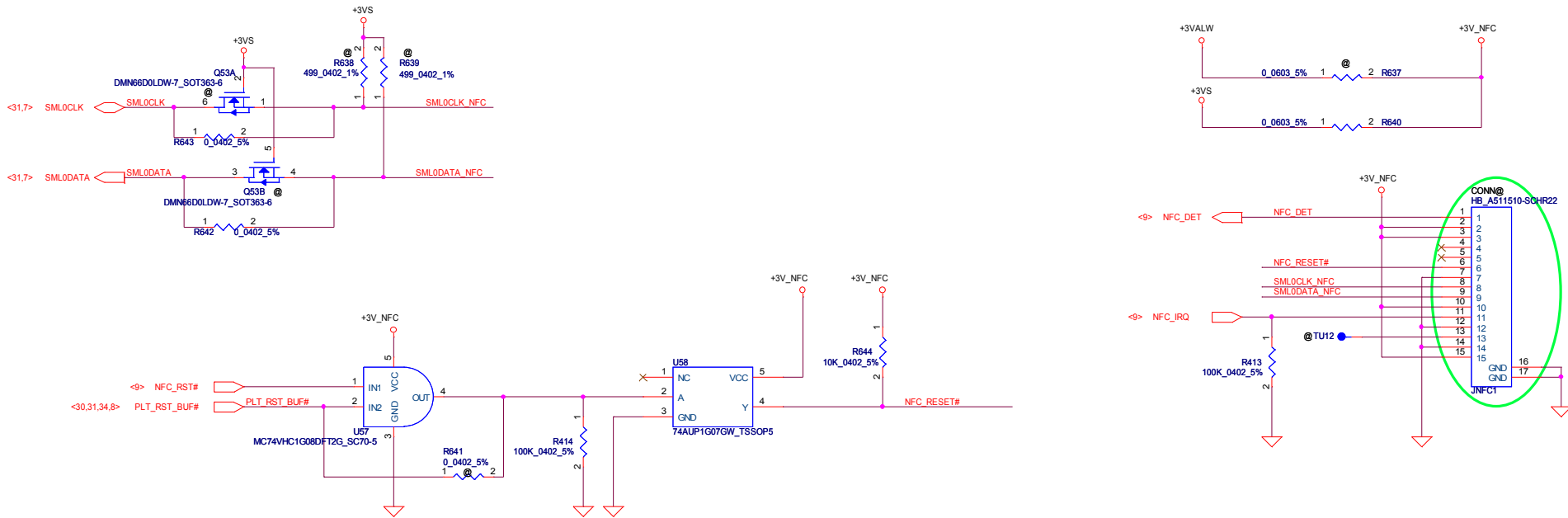
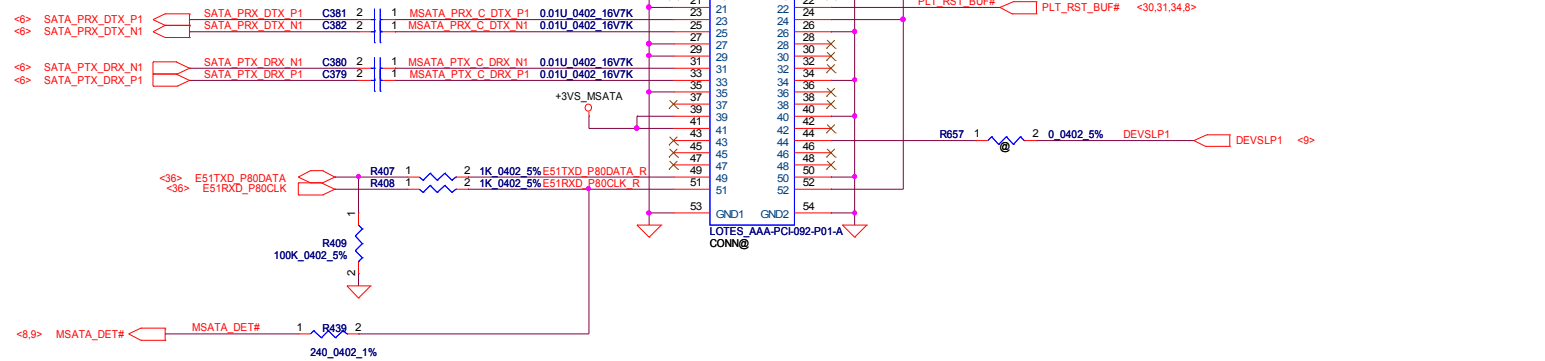


APS G-Sensor

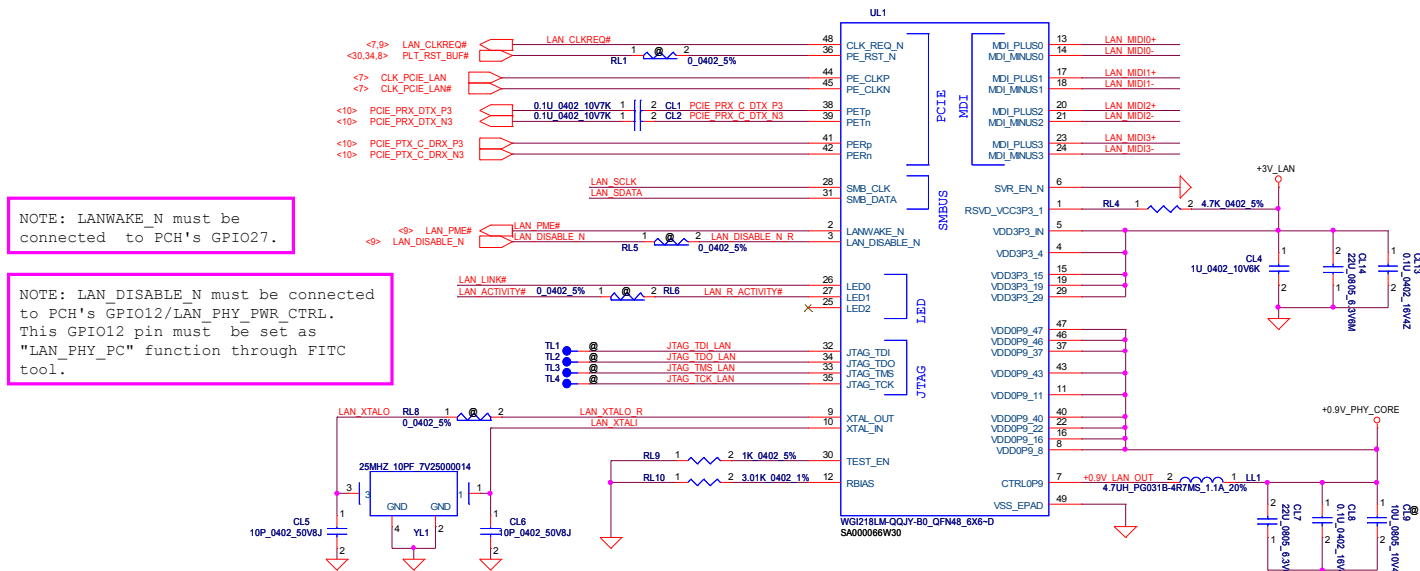


LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

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NOTE: LANWAKE_N must be connected to PCH's GPIO27.

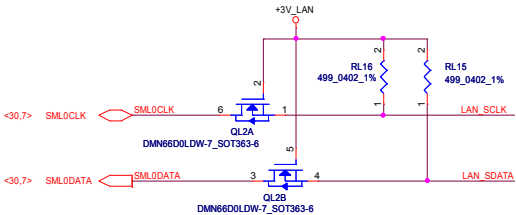
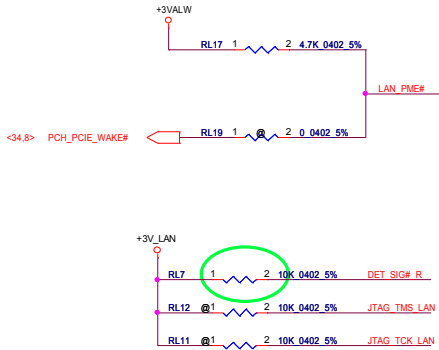
NOTE: LAN_DISABLE_N must be connected to PCH's GPIO12/LAN_PHY_PWR_CTRL. This GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

Connect RBIAS through a 3.01 kΩ 1% pull-down resistor to ground and then place it no more than one half inch (0.5") away from the PHY.

*IMPORTANT NOTE: LAN_PWR_EN Controls PHY Power

NOTE: Total requirement Cout>=20uF. ESR<50mohm.
LAYOUT NOTE: Place Ll1, CL7, CL8, CL9, and close to PHY

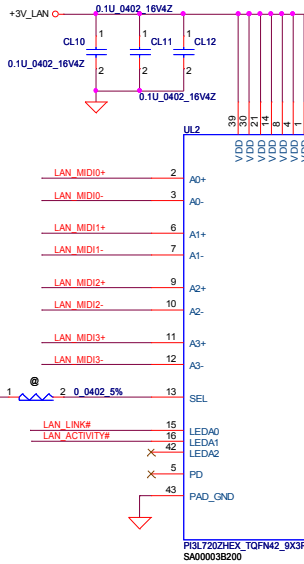
PD	SEL	Function
L	L	Ax to Bx; LEDAx to LEDBx
L	H	Ax to Cx; LEDAx to LEDCx
H	X	Hi-Z



NOTE: Default SMBus Address is 0xC8

SMBUS PULL-UP OPTIONS

SMBUS SPEED	RL15 & RL16
1MHz(Default setting)	499ohm
100KHz/400KHz	2.2Kohm

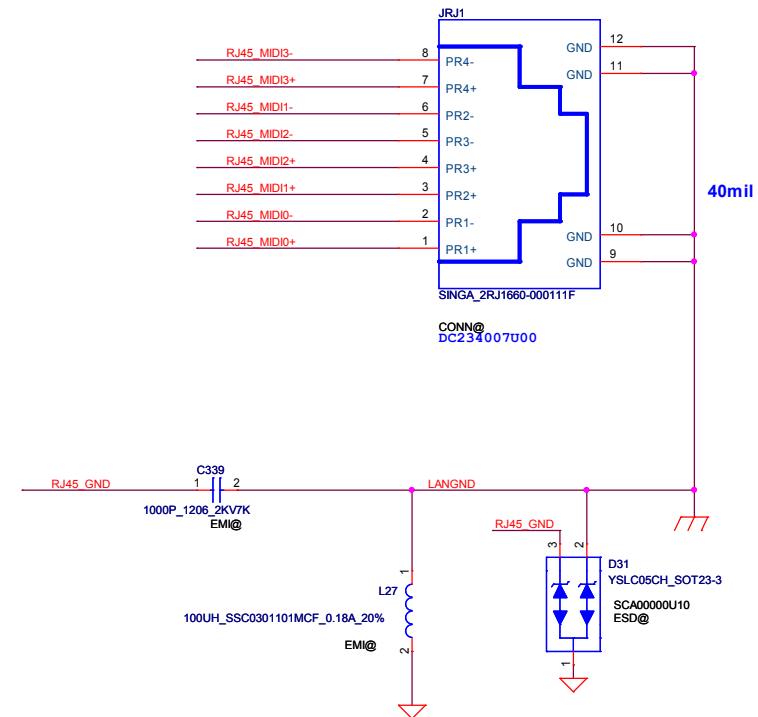
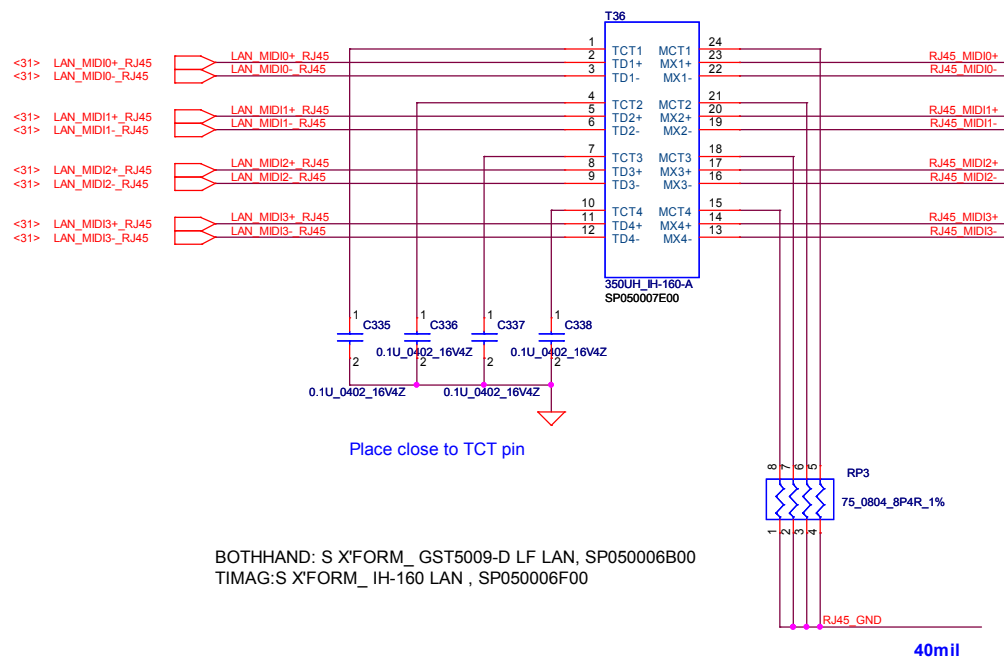


LAN Switch

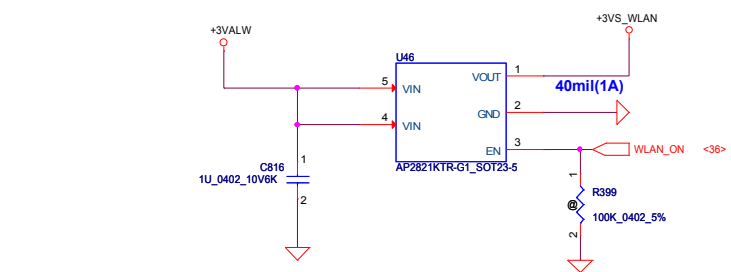
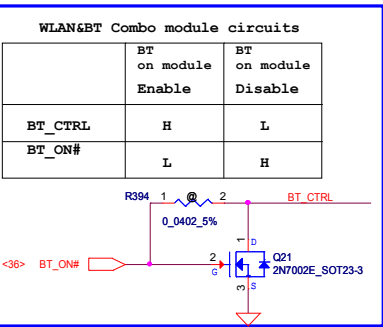
To Docking. SEL:Low

To RJ45 conn SEL:High

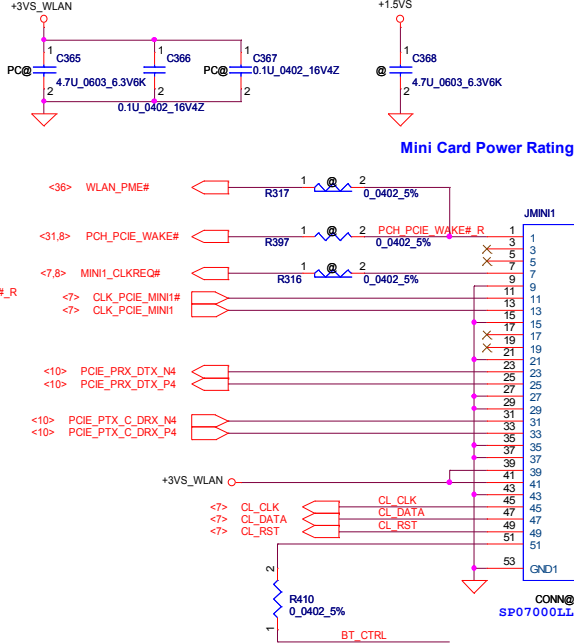
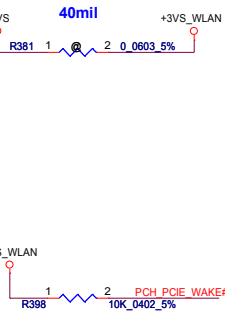
LAN Connector



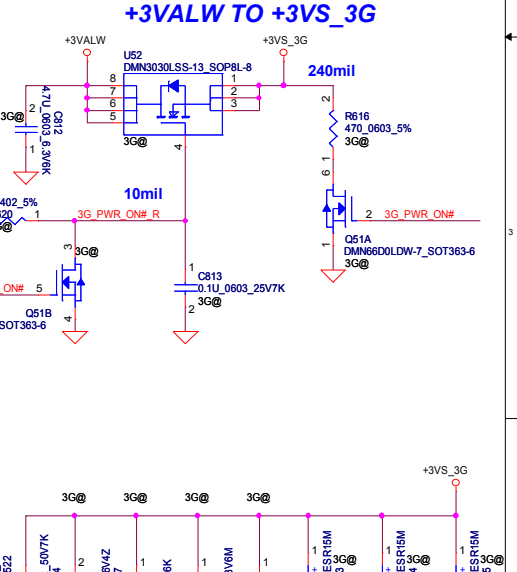
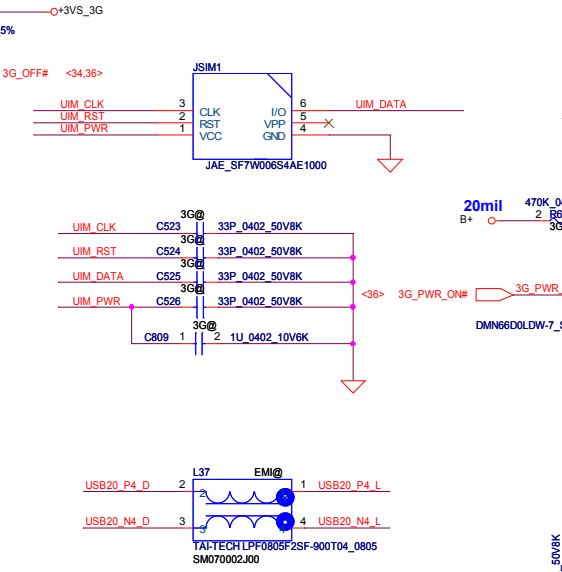
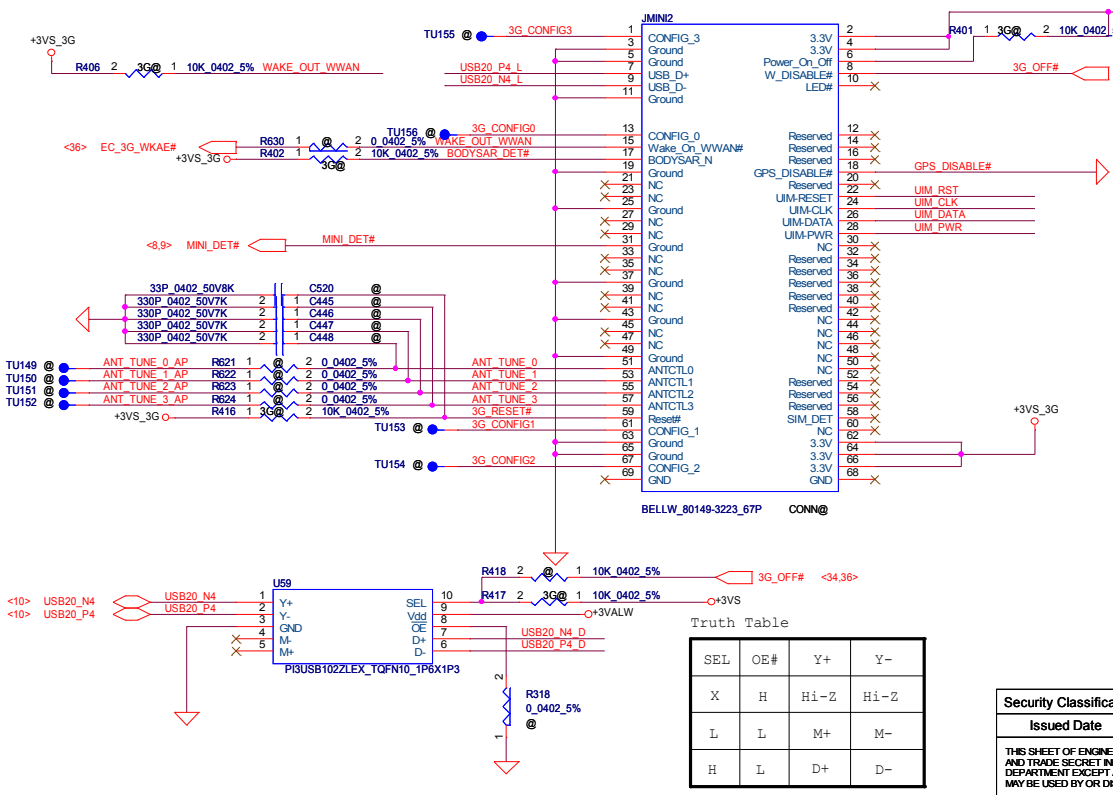
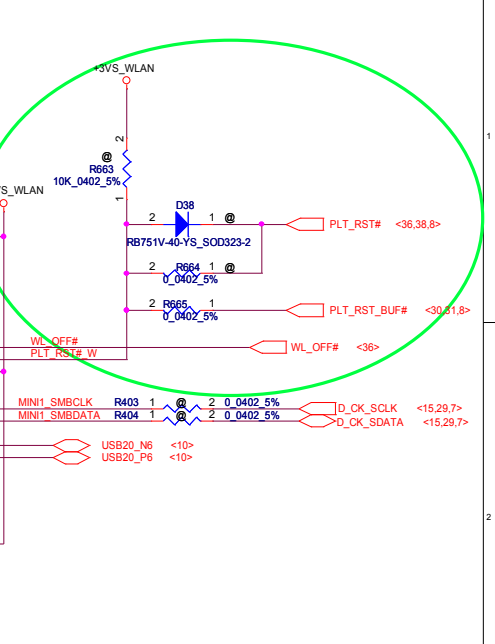
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				Size Custom	Document Number	Rev 1.0	
				V4DA2 M/B LA-A131P Schematic			
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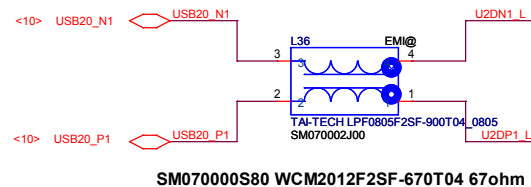


For Wireless LAN

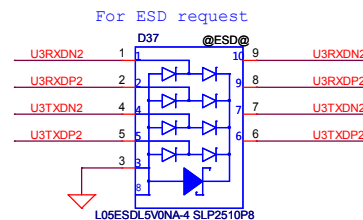
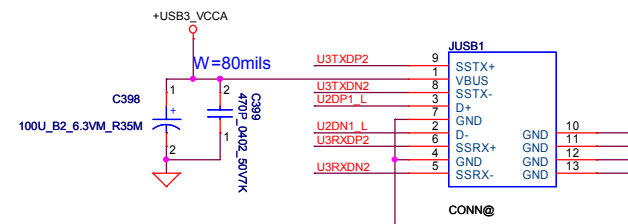
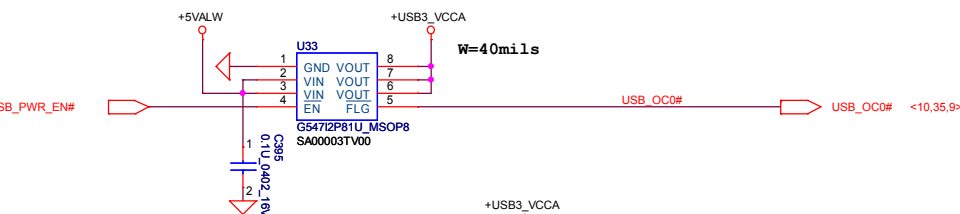
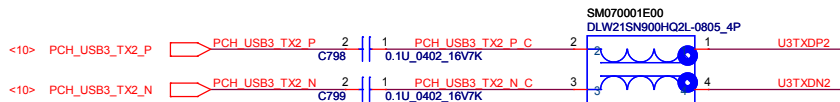
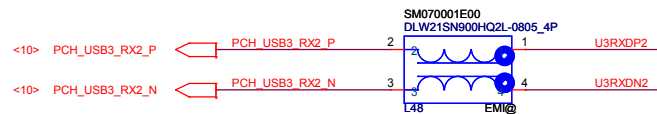


MINI CARD(Wireless LAN & BT)

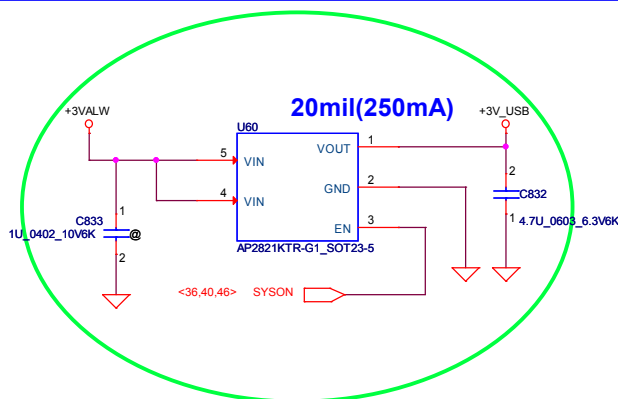




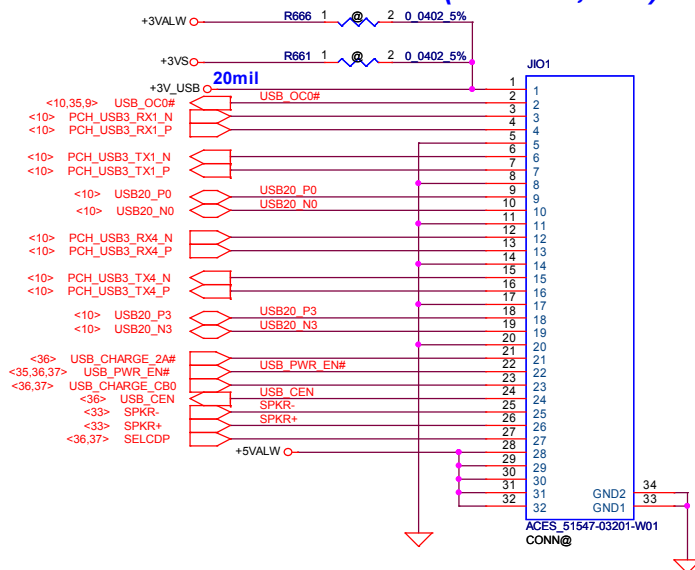
SM070000S80 WCM2012F2SF-670T04 67ohm



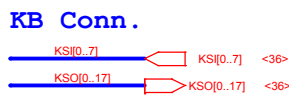
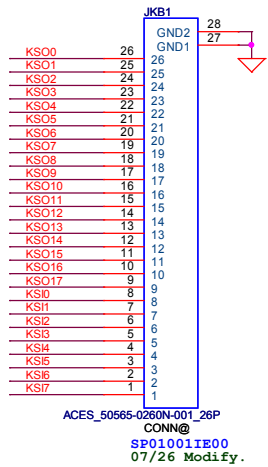
USB3.0 Conn.(MB)



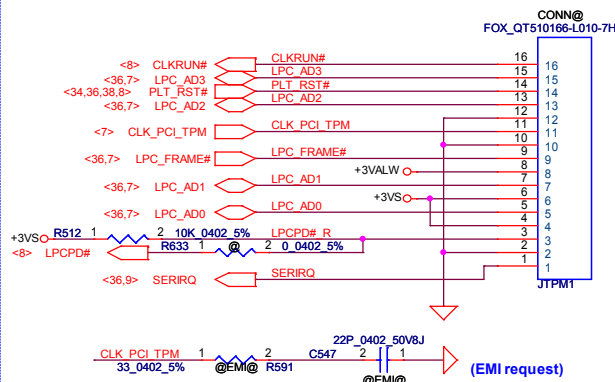
IO Board Conn(For FFC,FPC)



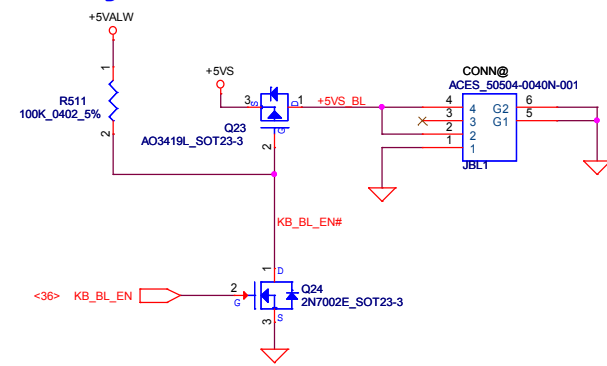
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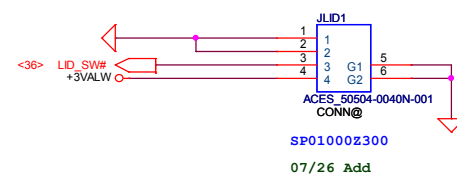
TPM Board



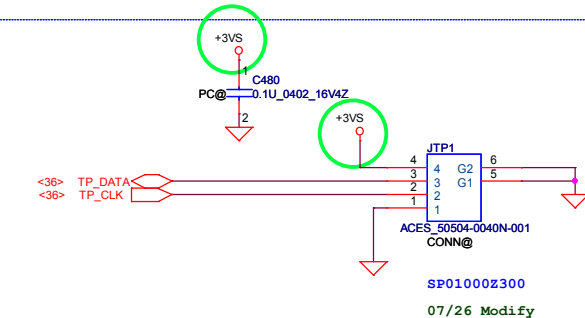
KB Backlight Conn



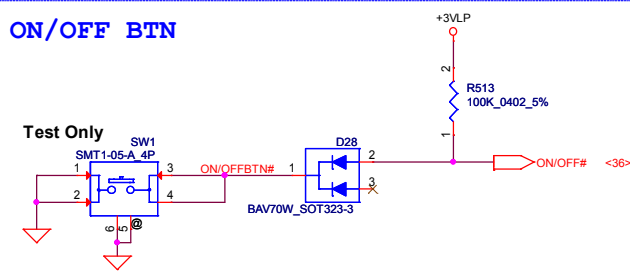
Lid Switch/B (Hall Effect Switch)



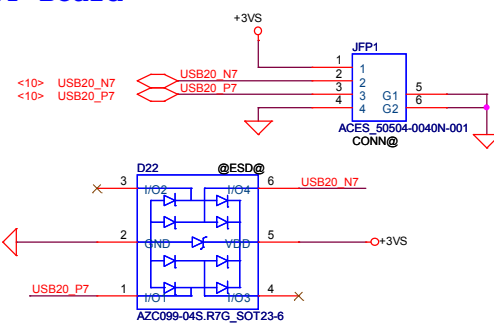
TP Conn.



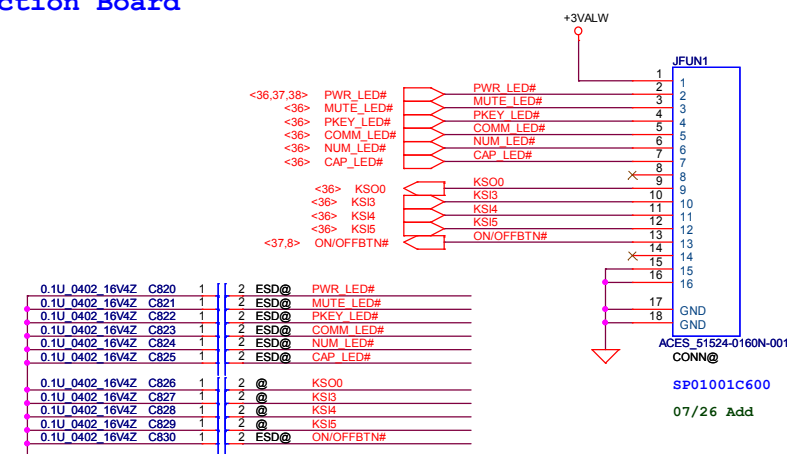
ON/OFF BTN



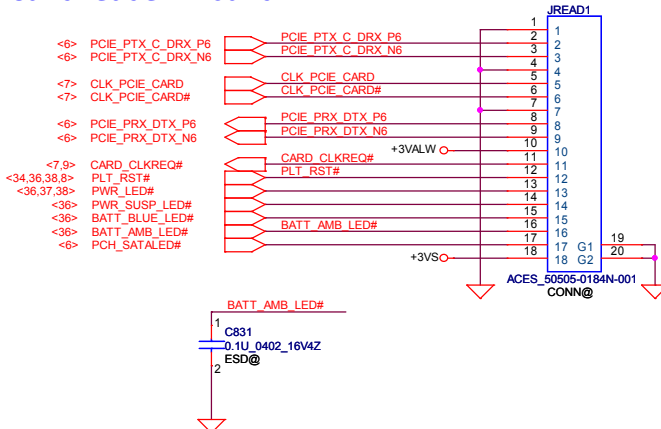
FP Board



Function Board

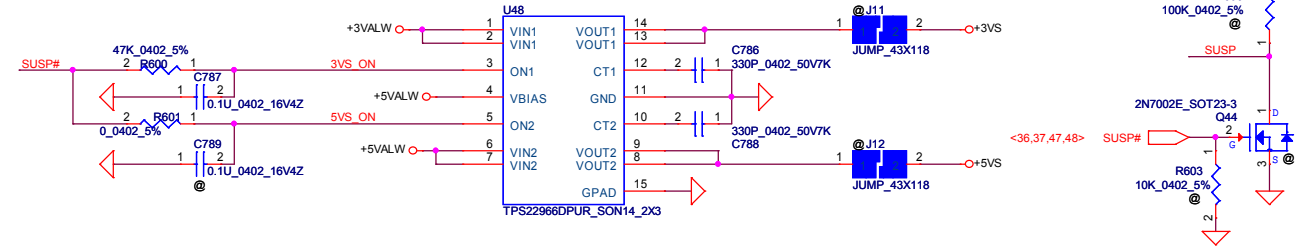
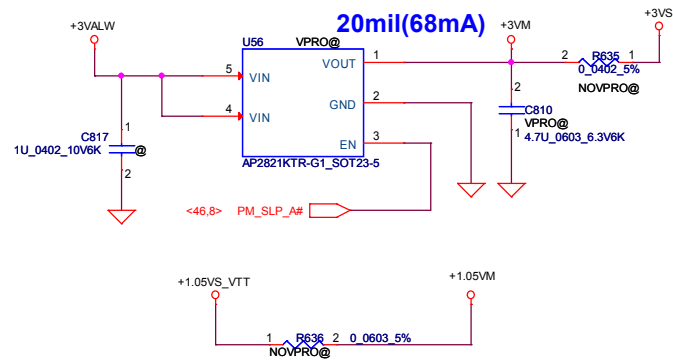


CardReader Board

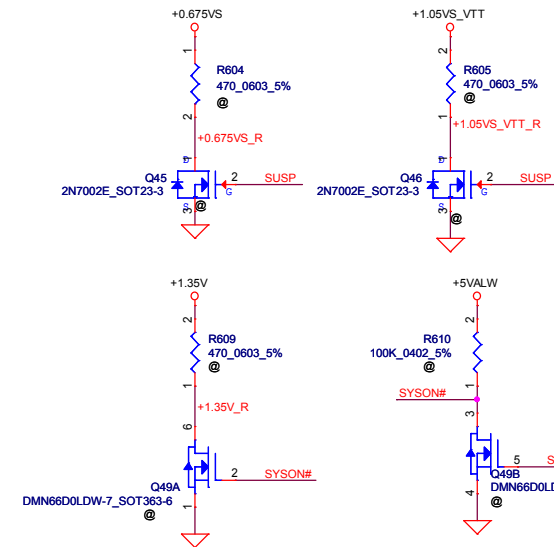
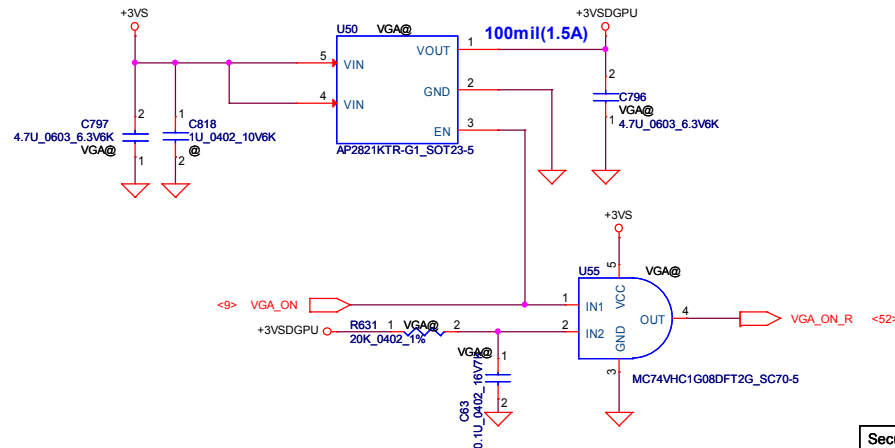


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+3VALW to +3VM for Intel AMT



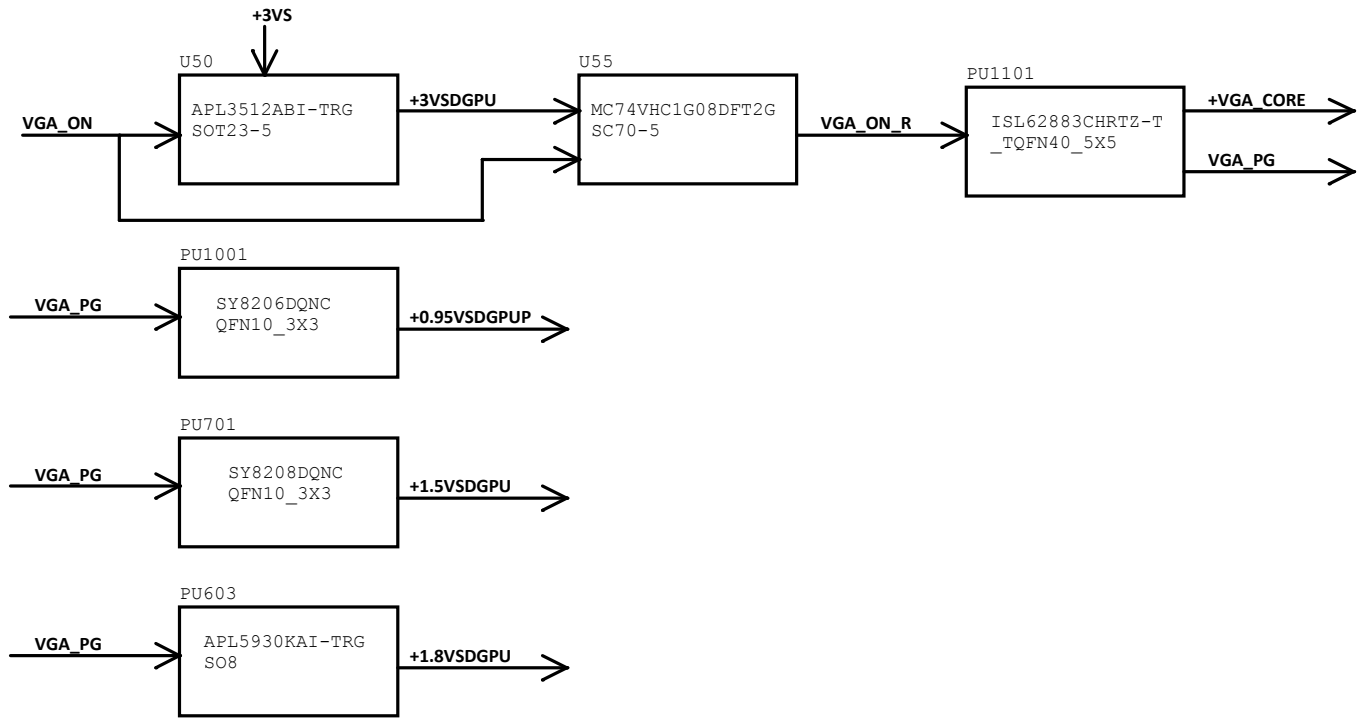
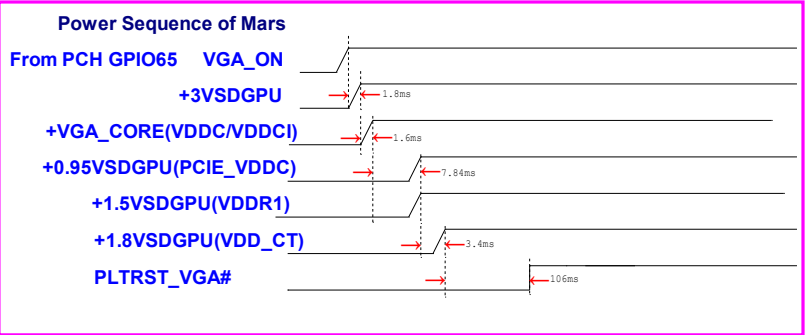
+3VS to +3VSDGPU for GPU



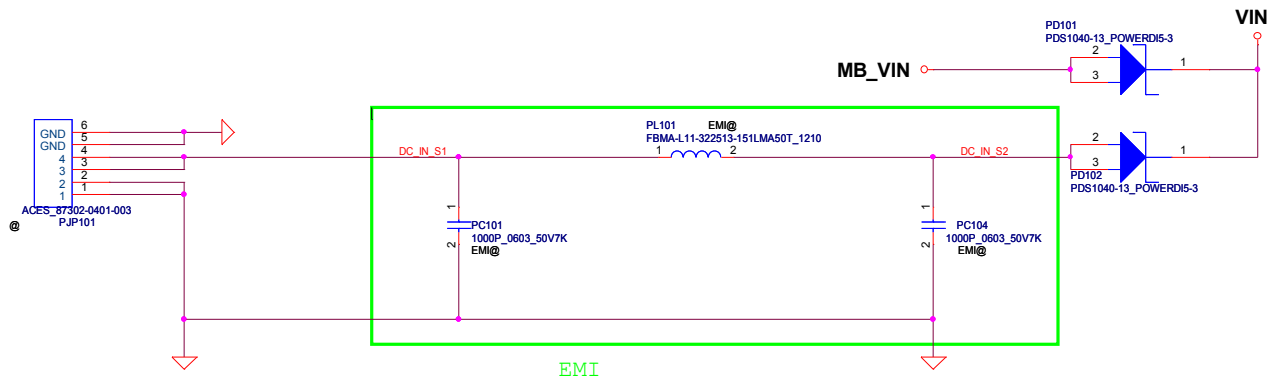
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						Size		Document Number			Rev	
						Custom		V4DA2 M/B LA-A131P Schematic			1.0	
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Power-Up/Down Sequence

- 1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- 2. VDD_CT must remain powered whenever VDDR3 is powered.
- 3. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
- 4. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).
- 5. BIF_VDDC should always be tied to PCIE_VDDC.

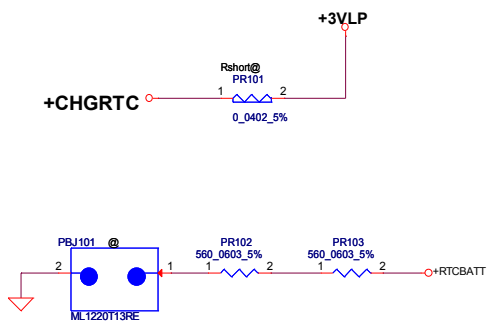


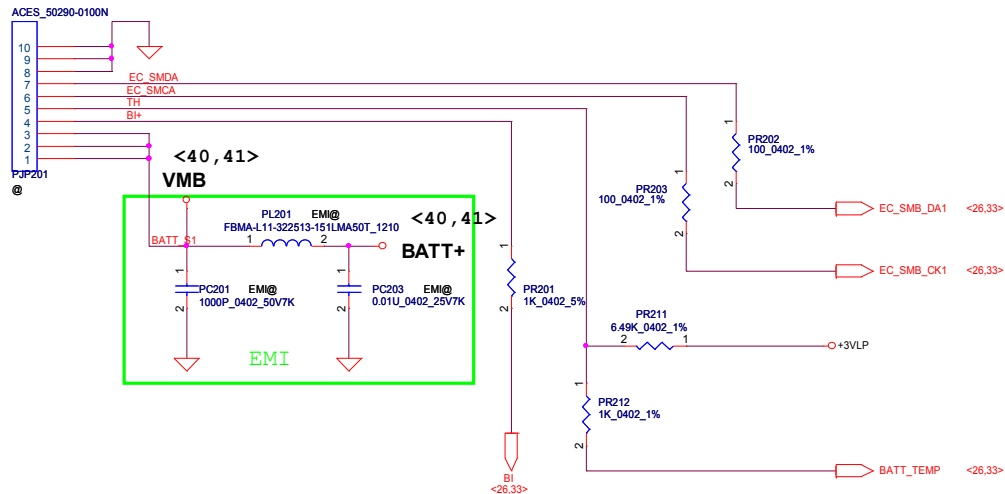
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Issued Date	2012/07/20	Deciphered Date	2013/07/20	Title		
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BOM Config

DDR3L	UMA	EMI@
	DIS	EMI@/VGA@/VGAEMI@





ENE9012	Action 70W (throttling)	Recovery 54W
ADP_I	1.466V	1.131V
VCIN1 (EC setting)	1.2V	1.025V

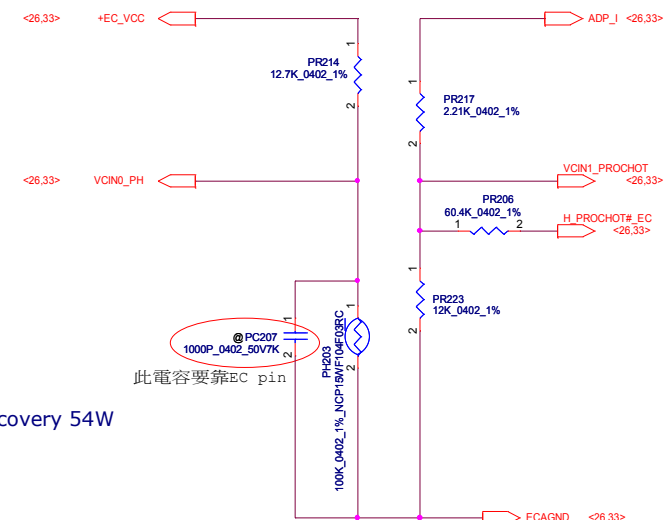
CPU thermal protection at 92 degree C

PH203 under CPU botten side :

(92 degree = 6.99K ohm) => VCIN0_PH = 1.2V

(56 degree = 26.02k ohm) => VCIN0_PH = 2.22V

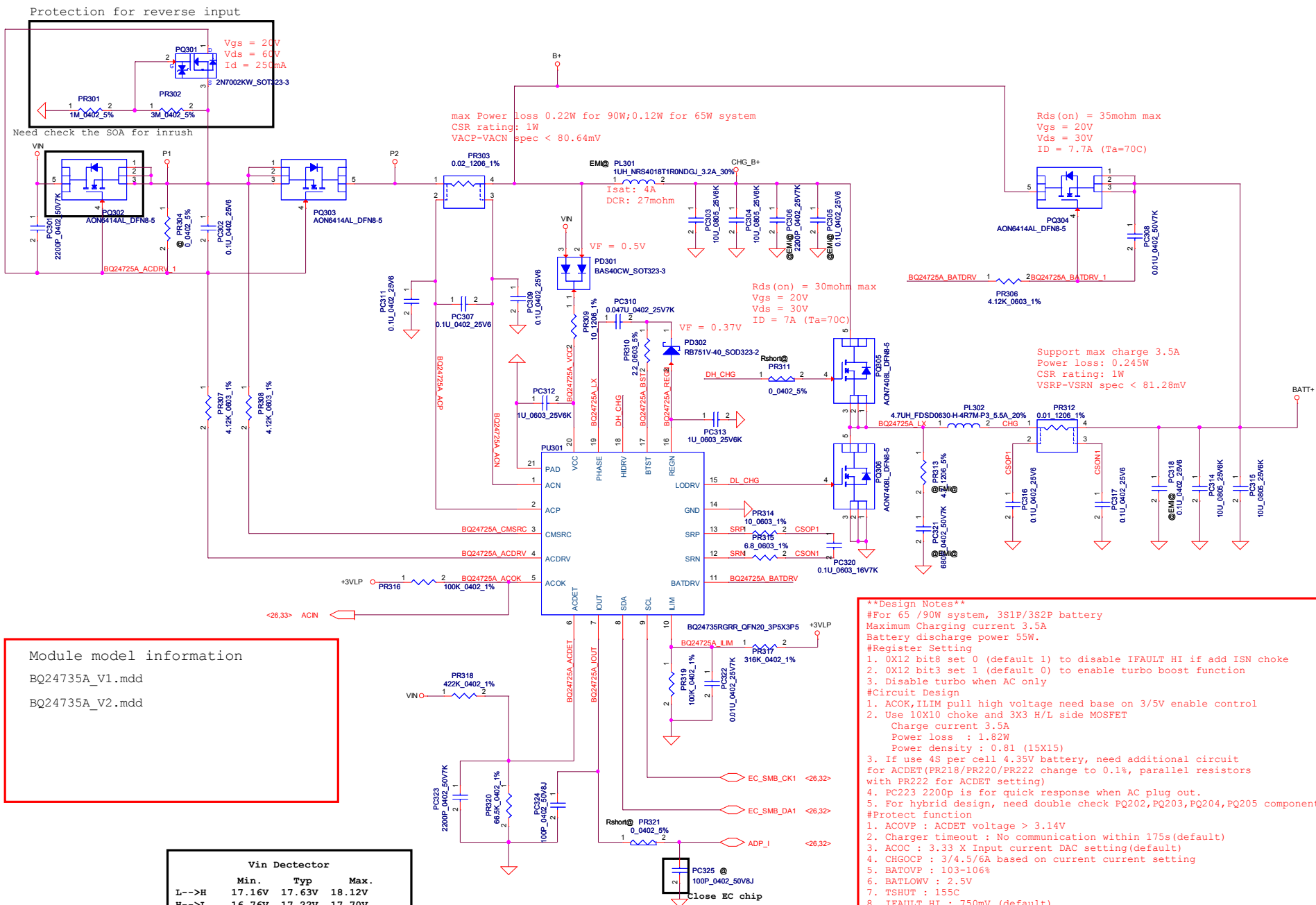
$(70W/19V) \times 19.9 \times 20m = 1.466V$
 $1.466 \times 10 / 12.21 = 1.2V$



此電容要靠EC pin

For 65W adapter==>action 70W , Recovery 54W

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****Design Notes****

#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Battery discharge power 55W.

#Register Setting

- 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
- 0X12 bit3 set 1 (default 0) to enable turbo boost function
- Disable turbo when AC only

#Circuit Design

- ACOK, ILIM pull high voltage need base on 3/5V enable control
- Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)
- If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
- PC223 2200p is for quick response when AC plug out.
- For hybrid design, need double check PQ202, PQ203, PQ204, PQ205 component rating

#Protect function

- ACOVLP : ACDET voltage > 3.14V
- Charger timeout : No communication within 175s(default)
- ACOC : 3.33 X Input current DAC setting(default)
- CHGOCP : 3/4.5/6A based on current current setting
- BATOVLP : 103-106%
- BATLOWV : 2.5V
- TSHUT : 155C
- IFAULT HI : 750mV (default)
- IFAULT LOW : 110mV (default)

SY8208B_V1.mdd



TDC=8A



SY8208C_V1.mdd

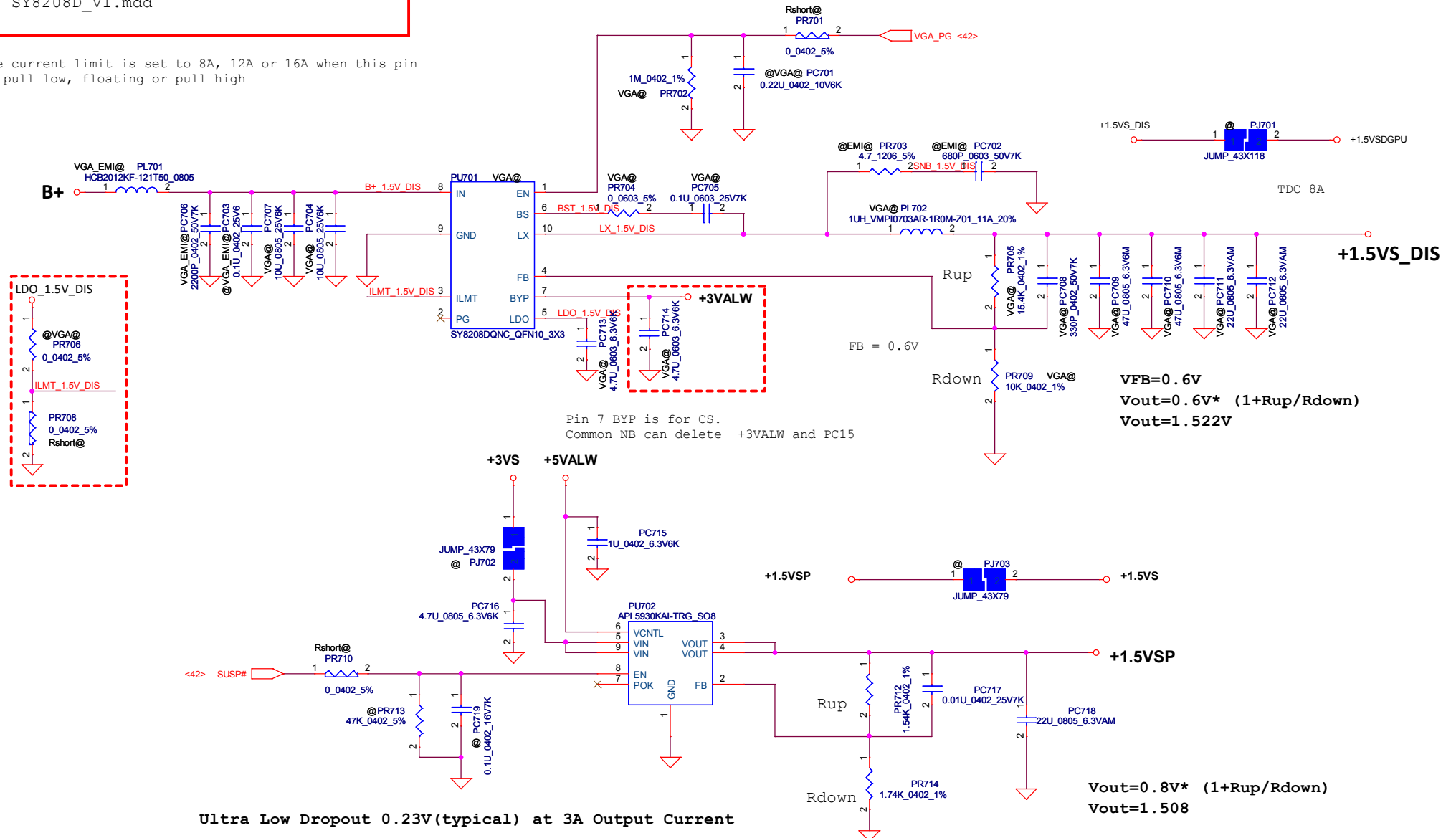
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> Title 3VALW/5VALW	
Issued Date	2012/06/19	Deciphered Date	2012/07/31		
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Module model information

SY8208D_V1.mdd

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

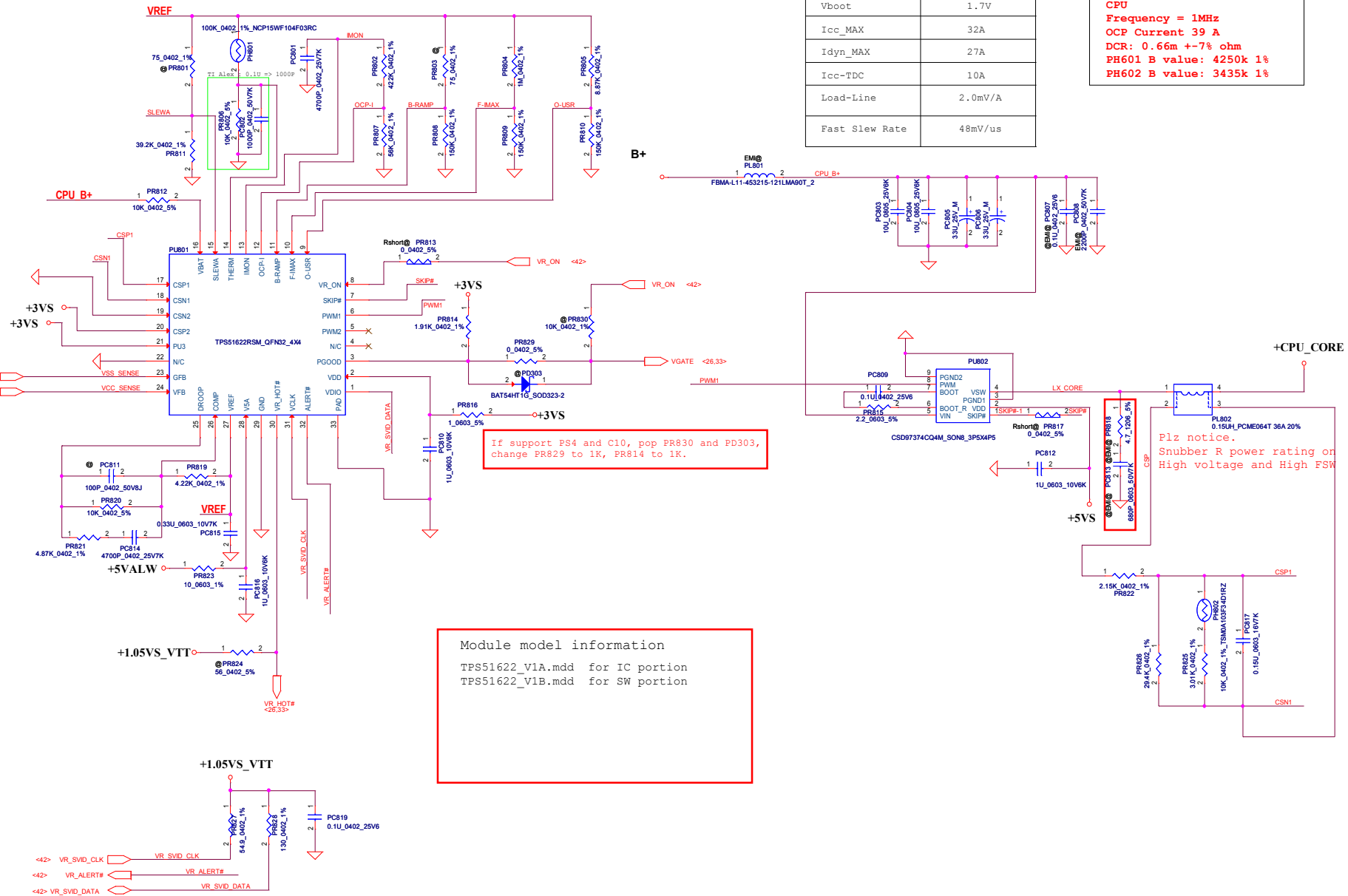


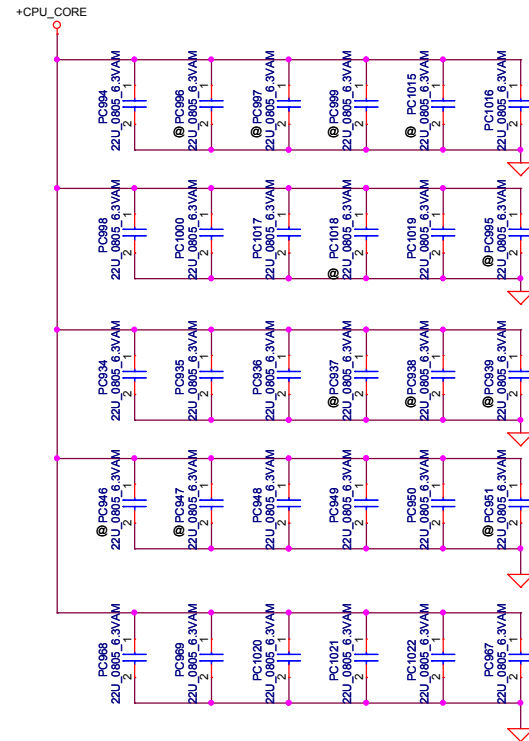
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				Document Number
				V4DA2 LAA131P Schematic
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VR_HOT#
PR806 10K ohm for 100 degree
PR806 8K ohm for 110 degree

Specifications	
Vps0	1.8V
Vboot	1.7V
Icc_MAX	32A
Idyn_MAX	27A
Icc-TDC	10A
Load-Line	2.0mV/A
Fast Slew Rate	48mV/us

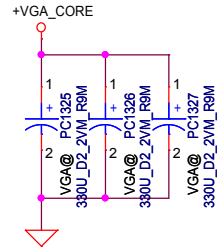
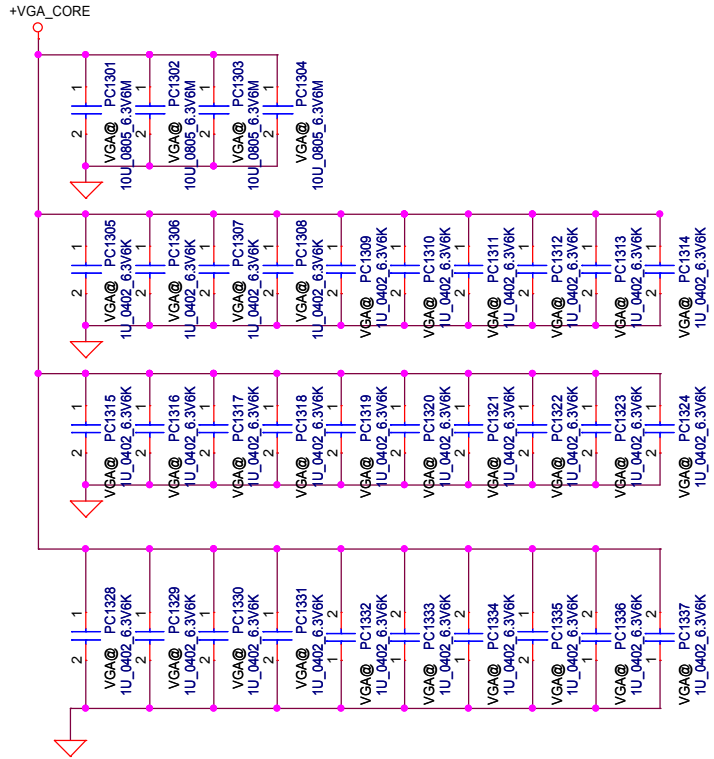
CPU
Frequency = 1MHz
OCP Current 39 A
DCR: 0.66m +/-7% ohm
PH601 B value: 4250k 1%
PH602 B value: 3435k 1%





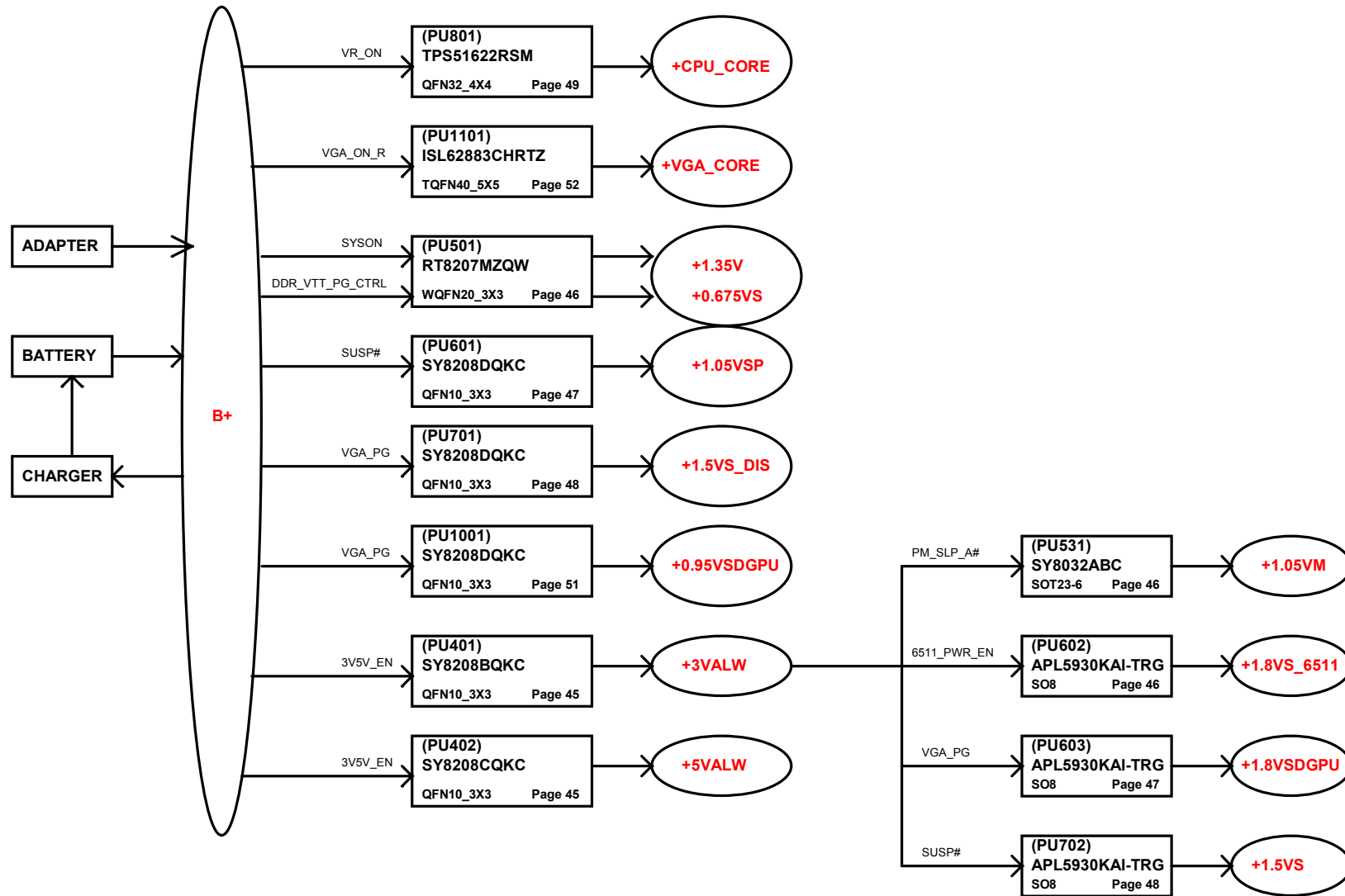
CPU LL=2m ohm dedign 22uF *18, 22uF*12(un-pop)

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AMD MARS
GPU_CORE
330uF*2
10uF*4+1uF*30

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				Custom	V4DA2 LAA131P Schematic	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		change Cff to 6.8nF of SY8208C (5V) and 10nF if SY8208B (3V). The 5VALW will fast than 3VALW and the rising time will under 2mS.	0.2	45	Change PC425 From SE075472K80 - 4700P 25V K X7R 0402 to SE075103K80 - .01U 25V K X7R 0402	20130426	DVT
02		change Cff to 6.8nF of SY8208C (5V) and 10nF if SY8208B (3V). The 5VALW will fast than 3VALW and the rising time will under 2mS.	0.2	45	Change PC426 From SE075472K80 - 4700P 25V K X7R 0402 to SE075682K80 - 6800P 25V K X7R 0402	20130426	DVT
03		modify 1.35VP output voltage from 1.515V modify to 1.355V	0.2	46	Change PR506 From SD028102280 - 10.2K +-1% 0402 to SD034806180 - 8.06K +-1% 0402	20130426	DVT
04		modify 1.05VMP output voltage from 1.2V modify to 1.0722V	0.2	46	Change PR533 From SD034200280 - 20K +-1% 0402 to SD034787180 - 7.87K +-1% 0402	20130426	DVT
05		modify 1.8VSP and 1.8VS_DIS output voltage from 1.508V modify to 1.839V	0.2	47	Change PR611, PR614 From SD034154180 - 1.54K +-1% 0402 to SD034226180 - 2.26K +-1% 0402	20130426	DVT
06		modify 1.5VSP output voltage from 1.05V modify to 1.5V	0.2	48	Change PR709 From SD034200280 - 20K +-1% 0402 to SD034100280 - 10K +-1% 0402	20130426	DVT
07		modify 0.95VSDGPUP output voltage from 1.05V modify to 0.972V	0.2	51	Change PR1006 From SD034150280 - 15K +-1% 0402 to SD00000AJ80 - 12.4K +-1% 0402	20130426	DVT
08		CPU_CORE choke DCR from 0.85m ohm adjust to 0.66m ohm, modify component to setting VREF, OCP,etc.	0.2	49	Change PR819 from SD034487100 - 4.87K +-1% 0402 to SD00000J280 - 4.32K +-1% 0402 Change PR826 from SD034200280 - 20K +-1% 0402 to SD034523280 - 52.3K +-1% 0402 Change PR822 from SD034226180 - 2.26K +-1% 0402 to D034210180 - 2.1K +-1% 0402 - Change PR807 from SD034390280 - 39K +-1% 0402 to SD034560280 - 56K +-1% 0402 Change PR802 from SD034365380 - 365K +-1% 0402 to SD034422300 - 442K +-1% 0402 Change PC817, PC818 to PC817 from SE076823K80 - 0.082U 16V K X7R 0402 to SE000000X80 0.15U 16V K X7R 0603	20130524	DVT
09		modify 1.05VSP output voltage from 1.05V modify to 1.062V for EA test voltage drop under 1.05V	0.2	47	Change PR636 From SD034150280 - 15K +-1% 0402 to SD034154280 - 15.4K +-1% 0402	20130524	DVT
10		modify 1.5VS_DIS output voltage from 1.5V modify to 1.522V for EA test voltage drop under 1.5V	0.2	48	Change PR705 From SD034150280 - 15K +-1% 0402 to SD034154280 - 15.4K +-1% 0402	20130524	DVT
11		modify VGA output capacitor from 560U*1+330U*2 reduce to 330U*3 static Pk-Pk ripple from 32.12mV up to 35.63mV dynamic Pk-Pk ripple from 88mV up to 94mV.	0.2	48	Change PC1327 From SGA00006J00 - 560U 2V M D2 LESR4.5M SX H1.9 to SGA00006100 - 330U 2V M D2 ESR9M S H1.9	20130524	DVT
12		modify 1.05VS/1.5VSDGPU/0.95VSDGPU choke from 1.5U change to 1U, for efficiency heavy load improve: 1.05V => from 83.2% to 85.5% 1.5V => from 83.7% to 85.5% 0.95V => from 80.6% to 84.8%	0.2	47, 48, 51	Change PL602, PL702, PL1002 From SH000008800 - 1.5UH +-20% PCMC063T-1R5MN 9A to SH00000KS00 - 1UH +-20% VMPI0703AR-1R0M-Z01 11A	20130524	DVT
13		Part count reduce PR609, PR612, PR710; PR615, PR616, PR713; PC621, PC622, PC719 are +1.5VS/1.8VS/1.8VSDGPU enable RC.	0.3	47, 48	Change PR609, PR612, PR710 change to Rshort8 From SD028100380-S RES 1/16W 100K +-5% 0402 to SD028000080-S RES 1/16W 0 +-5% 0402 Un-pop PR615, PR616, PR713 From SD028470280 - S RES 1/16W 47K +-5% 0402 to un-pop Un-pop PC621, PR622, PC719 From SE076104K80 - S CER CAP .1U 16V K X7R 0402 to un-pop	20130531	FVT
14		Part count reduce PR824 is VR-HOT# pull high resistor, beacuse there have a 0 ohm between VR_HOT# and H_PROCHOT#, H_PROCHOT# also have a pull high voltage, discuss with HW, we could un-pop PR824	0.3	49	Un-pop PR824 From SD028560A80 - S RES 1/16W 56 +-5% 0402 to un-pop	20130531	FVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
15		modify 1.35VP output voltage from 1.3515V modify to 1.365V	0.3	46	Change PR506 From SD034806180 - 8.06K +-1% 0402 to SD000004100 - 8.2K +-1% 0402	20130606	PVT
16		part count reduce	0.3	45 47 51	Change PR401, PR409, PR634, PR1004 From SD013000080 - 0_0603_5% to R_short	20130606	PVT
17		part count reduce	0.3	44,46 47,48 51,52	Change PR311, PR534, PR631, PR635, PR701, PR706, PR1001, PR1008, PR1115, PR1150, PR1154, PR1155, PR1156 From SD028000080 - 0_0402_5% to R_short	20130606	PVT
18	PS51622 which might cause system hang when exit C10 with PS4. TI solution : RC filter to ignore the ~4us glitch on PGOOD.	TI suggest, If support PS4 and C10, pop PR830 and PD303, change PR829 to 1K, PR814 to 1K.	0.3	49	reserve PD303, SCS00003M00 - SCH DIO BAT54HT1G SOD323 reserve PR830, SD034100280 - 10K +-1% 0402 Add PR829, SD034100180 - 0 +-5% 0402	20130628	PVT
19		MOS AON7702A EOL	0.3	46	Change PQ502 from SB00000T600 - AON7702A 1N DFN to SB000010A00 - AON7506 1N DFN	20130628	PVT
20		Finetune RC for CPU Transient Voltage Testing	0.3	49	Change PR819 from SD00000J280 - 4.32K +-1% 0402 to SD034422180 - 4.22K +-1% 0402 Change PR822 from SD034210180 - 2.1K +-1% 0402 to SD034215180 - 2.15K +-1% 0402 Change PR826 from SD034523280 - 52.3K +-1% 0402 to SD034294280 - 29.4K +-1% 0402 Change PR802 from SD034442300 - 442K +-1% 0402 to SD034422380 - 422K +-1% 0402	20130628	PVT
21		part count reduce output capacitor reference CPU Transient Voltage Testing	0.3	49	Change PC1005, PC938, PC939, PC946, PC951, PC997 from SE000008L80 - CER CAP 22U 6.3V M X6S 0805 H1.25 to un-pop	20130628	PVT
22		EMT test 5V and 1.05VS, Main source SY8208C/D could PASS, but 2nd source SY8206C/D fail, EMI add snubber the both could PASS.	0.4	45, 47	Add EMI solution Snubber at 5V and 1.05VS PC424 680pF, PC632 680pF PR410 4.7 ohm, PR633 4.7 ohm	20130731	PVT2/ Pre-MP
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EVT-->DVT Change List

- 1.page36, pin 68 and pin 21 SWAP and pin 89 and pin 17
- 2.page30, R407,R408,change to 1K and R439 connect to JMINI3.51 and R439 change to 240 ohm
- 3.page28, R478, R482 change to mount
- 4.page39, R527 change to 1M
- 5.page33, R592 and R593 change to 60.4 ohm
- 6.page27, remove C248,C253,C404,C405,QA2,RA5,RA6,RA7,RA8,U45
- update U11 and add T39
- add R645 ,R646 ,L12,L13
- U11.16 connect to +5VS
- C782 connect to +5VS
- add R647 and R648
- R647 and R648 change to @
- R645 ,R646 change to SD028100A80
- C249 and C251 change to mount
- 7.page26, RA12 and RA14 mount ,RA16 and RA18 un-mount
- RA2,RA3,RA4,RA9 mount
- RA32 change to 93.1 ohm
- CA22 and CA21 change to SE071150J80
- 8.page30, JNFC1.15 connect to GPIO 17
- R637 change to unmount ,R640 change to mount
- 9.page37, add C814 and C814 change to 1UF
- 10.page30, JMINI3.44 connect to UU1.L2 and add R657 ,R658
- 11.page32, T36 change PN to SP050007E00
- 12.page34, R620 change to 470K
- ESD modify
- 1.page37, add R649~R656

DVT-->PVT Change List

- 1.page36, remove JIO2
- 2.page27, L6,L8,L10,L12,L13 from SM01000GA00 change to SM01000FH00 for downsize of source suggest
- 3.page36, L40,L41,L44,L45,L46,L47 from SM010015410 to SM01000N000 for downsize of source suggest
- 4.page33, L31 from SM010017710 to SM01000FH00 for downsize of source suggest
- 5.page26, LA2 from SM010030010 to SM010028100 for downsize of source suggest
- 6.page19,21 LV1,LV2,LV3,LV7,LV8,LV9 from SM010030010 to SM010028100 for downsize of source suggest
- 7.page25, U44 from SA00003AR00 to SA00006EE00 for cost down
- 8.page34, U46 from SA00003AR00 to SA00006EE00 for cost down
- 9.page40, U50 and U56 from SA00003AR00 to SA00006EE00 for cost down
- 10.page31, UL3 from SA00003AR00 to SA00006EE00 for cost down
- 11.page37, C814 change to SE000000K80 for downsize
- 12.page33, add R659 and R660 for audio suggest
- 13.page27, R645 and R646 change to 33 ohm for CRT overshoot
- 14.page33, L31 change to SM01000II00 for downsize of source suggest
- 15.page38, update JLID1 pin define
- 16.page34, update C803 ,C804,C805 SN to SGA00000Y80
- ESD modify
- 1.page38 add 831
- 2.page38 add C820~830
- 3.page15 add CU186 (@ESD@)
- 4.page8, add CU187 (@ESD@)

PVT-->Per-MP Change List

- 1.page30, JNFC1 SWAP
- 2.page38, C480 and JTP1.4 connect to +3VS
- 3.page8, JAPS.11 connect to ON/OFFBTN#
- 4.page31,add RU176 to @
- 5.page9, RPU19.8 and UU1.AG5 connect to DET_SIG#_R_1
- 6.page9, add RU176
- 7.page35, JIO1.1 connect to +3VALW and reserve +3VS ,add R661 and R662
- 8.page27, L6,L8,L10,L12,L13 from SM01000FH00 change to SM01000GA00
- 9.page35, add U60 ,C833, C832 ,R666,R661
- 10.page34, add R664 ,D38,R663
- 11.page33, R659 and R660 change to 0 ohm
- 12.page38, C826~C829 change to @
- 13.page36, L40 and L41 change to SM01000DS00 (NBQ100505T-800Y)
- 14.page33, L44~L47 change to SM01000DS00 (NBQ100505T-800Y)
- 15.page36, R483 change to 20K
- 16.page38, SW1 to @
- 17.page39, SW3 to @
- 18.page7, add second source
- 19.page28, R478 un-mount ,R448 mount

Title			
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